INTRODUCTION TO POWER ELECTRONICS

Power Electronics is a field which combines Power (electric power), Electronics and Control systems.

Power engineering deals with the static and rotating power equipment for the generation, transmission and distribution of electric power.

Electronics deals with the study of solid state semiconductor power devices and circuits for Power conversion to meet the desired control objectives (to control the output voltage and output power).

Power electronics may be defined as the subject of applications of solid state power semiconductor devices (Thyristors) for the control and conversion of electric power.

Power electronics deals with the study and design of Thyristorised power controllers for variety of application like Heat control, Light/Illumination control, Motor control – AC/DC motor drives used in industries, High voltage power supplies, Vehicle propulsion systems, High voltage direct current (HVDC) transmission.

BRIEF HISTORY OF POWER ELECTRONICS

The first Power Electronic Device developed was the Mercury Arc Rectifier during the year 1900. Then the other Power devices like metal tank rectifier, grid controlled vacuum tube rectifier, igniton, phanotron, thyatron and magnetic amplifier, were developed & used gradually for power control applications until 1950.

The first SCR (silicon controlled rectifier) or Thyristor was invented and developed by Bell Lab’s in 1956 which was the first PNPN triggering transistor.

The second electronic revolution began in the year 1958 with the development of the commercial grade Thyristor by the General Electric Company (GE). Thus the new era of power electronics was born. After that many different types of power semiconductor devices & power conversion techniques have been introduced. The power electronics revolution is giving us the ability to convert, shape and control large amounts of power.

SOME APPLICATIONS OF POWER ELECTRONICS

Advertising, air conditioning, aircraft power supplies, alarms, appliances – (domestic and industrial), audio amplifiers, battery chargers, blenders, blowers, boilers, burglar alarms, cement kiln, chemical processing, clothes dryers, computers, conveyors, cranes and hoists, dimmers (light dimmers), displays, electric door openers, electric dryers, electric fans, electric vehicles, electromagnets, electro mechanical electro plating, electronic ignition, electrostatic precipitators, elevators, fans, flashers, food mixers, food warmer trays, fork lift trucks, furnaces, games, garage door openers, gas turbine starting, generator exciters, grinders, hand power tools, heat controls, high frequency lighting, HVDC transmission, induction heating, laser power supplies, latching relays, light flashers, linear induction motor controls, locomotives, machine tools, magnetic recording, magnets, mass transit railway system, mercury arc lamp ballasts, mining, model trains, motor controls, motor drives, movie projectors, nuclear reactor control rod, oil well drilling, oven controls, paper mills, particle accelerators, phonographs, photo copiers, power suppliers, printing presses, pumps and compressors, radar/sonar power supplies, refrigerators, regulators, RF amplifiers, security systems, servo systems, sewing machines, solar power supplies, solid-state contactors, solid-state relays, static circuit breakers, static relays, steel mills, synchronous motor starting, TV circuits, temperature controls, timers and toys, traffic signal controls, trains, TV deflection circuits, ultrasonic...
generators, UPS, vacuum cleaners, VAR compensation, vending machines, VLF transmitters, voltage regulators, washing machines, welding equipment.

**POWER ELECTRONIC APPLICATIONS**

**COMMERCIAL APPLICATIONS**

**DOMESTIC APPLICATIONS**
Cooking Equipments, Lighting, Heating, Air Conditioners, Refrigerators & Freezers, Personal Computers, Entertainment Equipments, UPS.

**INDUSTRIAL APPLICATIONS**

**AEROSPACE APPLICATIONS**
Space shuttle power supply systems, satellite power systems, aircraft power systems.

**TELECOMMUNICATIONS**
Battery chargers, power supplies (DC and UPS), mobile cell phone battery chargers.

**TRANSPORTATION**
Traction control of electric vehicles, battery chargers for electric vehicles, electric locomotives, street cars, trolley buses, automobile electronics including engine controls.

**UTILITY SYSTEMS**
High voltage DC transmission (HVDC), static VAR compensation (SVC), Alternative energy sources (wind, photovoltaic), fuel cells, energy storage systems, induced draft fans and boiler feed water pumps.

**POWER SEMICONDUCTOR DEVICES**
- Power Diodes.
- Power Transistors (BJT’s).
- Power MOSFETS.
- IGBT’s.
- Thyristors
  Thrystors are a family of p-n-p-n structured power semiconductor switching devices
- SCR’s (Silicon Controlled Rectifier)
  The silicon controlled rectifier is the most commonly and widely used member of the thyristor family. The family of thyristor devices include SCR’s, Diacs, Triacs, SCS, SUS, LASCAR’s and so on.
POWER SEMICONDUCTOR DEVICES USED IN POWER ELECTRONICS

The first thyristor or the SCR was developed in 1957. The conventional Thyristors (SCR’s) were exclusively used for power control in industrial applications until 1970. After 1970, various types of power semiconductor devices were developed and became commercially available. The power semiconductor devices can be divided broadly into five types

- Power Diodes.
- Thyristors.
- Power BJT's.
- Power MOSFET’s.
- Insulated Gate Bipolar Transistors (IGBT’s).
- Static Induction Transistors (SIT’s).

The Thyristors can be subdivided into different types

- Forced-commutated Thyristors (Inverter grade Thyristors)
- Line-commutated Thyristors (converter-grade Thyristors)
- Gate-turn off Thyristors (GTO).
- Reverse conducting Thyristors (RCT’s).
- Static Induction Thyristors (SITH).
- Gate assisted turn-off Thyristors (GATT).
- Light activated silicon controlled rectifier (LASC R) or Photo SCR’s.
- MOS-Controlled Thyristors (MCT’s).

POWER DIODES

Power diodes are made of silicon p-n junction with two terminals, anode and cathode. P-N junction is formed by alloying, diffusion and epitaxial growth. Modern techniques in diffusion and epitaxial processes permit desired device characteristics.

The diodes have the following advantages

- High mechanical and thermal reliability
- High peak inverse voltage
- Low reverse current
- Low forward voltage drop
- High efficiency
- Compactness.

Diode is forward biased when anode is made positive with respect to the cathode. Diode conducts fully when the diode voltage is more than the cut-in voltage (0.7 V for Si). Conducting diode will have a small voltage drop across it.

Diode is reverse biased when cathode is made positive with respect to anode. When reverse biased, a small reverse current known as leakage current flows. This leakage current increases with increase in magnitude of reverse voltage until avalanche voltage is reached (breakdown voltage).
DYNAMIC CHARACTERISTICS OF POWER SWITCHING DIODES

At low frequency and low current, the diode may be assumed to act as a perfect switch and the dynamic characteristics (turn on & turn off characteristics) are not very important. But at high frequency and high current, the dynamic characteristics plays an important role because it increases power loss and gives rise to large voltage spikes which may damage the device if proper protection is not given to the device.

The waveform in
(a) Simple diode circuit.
(b) Input waveform applied to the diode circuit in (a);
(c) The excess-carrier density at the junction;
(d) the diode current;
(e) the diode voltage.

Fig: Storage & Transition Times during the Diode Switching
**REVERSE RECOVERY CHARACTERISTIC**

Reverse recovery characteristic is much more important than forward recovery characteristics because it adds recovery losses to the forward loss. Current when diode is forward biased is due to net effect of majority and minority carriers. When diode is in forward conduction mode and then its forward current is reduced to zero (by applying reverse voltage) the diode continues to conduct due to minority carriers which remains stored in the p-n junction and in the bulk of semi-conductor material. The minority carriers take some time to recombine with opposite charges and to be neutralized. This time is called the **reverse recovery time**. The reverse recovery time ($t_{rr}$) is measured from the initial zero crossing of the diode current to 25% of maximum reverse current $I_{rr}$. $t_{rr}$ has 2 components, $t_1$ and $t_2$. $t_1$ is as a result of charge storage in the depletion region of the junction i.e., it is the time between the zero crossing and the peak reverse current $I_{rr}$. $t_2$ is as a result of charge storage in the bulk semi-conductor material.

\[
I_{rr} = t_1 + t_2 \\
I_{rr} = t_1 \left(\frac{di}{dt}\right)
\]

The reverse recovery time depends on the junction temperature, rate of fall of forward current and the magnitude of forward current prior to commutation (turning off). When diode is in reverse biased condition the flow of leakage current is due to minority carriers. Then application of forward voltage would force the diode to carry current in the forward direction. But a certain time known as forward recovery time (turn-ON time) is required before all the majority carriers over the whole junction can contribute to current flow. Normally forward recovery time is less than the reverse recovery time. The forward recovery time limits the rate of rise of forward current and the switching speed.

**Reverse recovery charge** $Q_{rr}$, is the amount of charge carriers that flow across the diode in the reverse direction due to the change of state from forward conduction to reverse blocking condition. The value of reverse recovery charge $Q_{rr}$ is determined form the area enclosed by the path of the reverse recovery current.

\[
Q_{rr} = \frac{1}{2} I_{rr} t_1 + \frac{1}{2} I_{rr} t_2 = \frac{1}{2} I_{rr} t_{rr'} \\
\therefore Q_{rr} = \frac{1}{2} I_{rr} t_{rr'}
\]
POWER DIODES TYPES

Power diodes can be classified as

- General purpose diodes.
- High speed (fast recovery) diodes.
- Schottky diode.

GENERAL PURPOSE DIODES

The diodes have high reverse recovery time of about 25 microsec (μsec). They are used in low speed (frequency) applications. e.g., line commutated converters, diode rectifiers and converters for a low input frequency upto 1 KHz. Diode ratings cover a very wide range with current ratings less than 1 A to several thousand amps (2000 A) and with voltage ratings from 50 V to 5 KV. These diodes are generally manufactured by diffusion process. Alloyed type rectifier diodes are used in welding power supplies. They are most cost effective and rugged and their ratings can go upto 300A and 1KV.

FAST RECOVERY DIODES

The diodes have low recovery time, generally less than 5 μs. The major field of applications is in electrical power conversion i.e., in free-wheeling ac-dc and dc-ac converter circuits. Their current ratings is from less than 1 A to hundreds of amperes with voltage ratings from 50 V to about 3 KV. Use of fast recovery diodes are preferable for free-wheeling in SCR circuits because of low recovery loss, lower junction temperature and reduced $di/dt$. For high voltage ratings greater than 400 V they are manufactured by diffusion process and the recovery time is controlled by platinum or gold diffusion. For less than 400 V rating epitaxial diodes provide faster switching speeds than diffused diodes. Epitaxial diodes have a very narrow base width resulting in a fast recovery time of about 50 ns.

SCHOTTKY DIODES

A Schottky diode has metal (aluminium) and semi-conductor junction. A layer of metal is deposited on a thin epitaxial layer of the n-type silicon. In Schottky diode there is a larger barrier for electron flow from metal to semi-conductor.

When Schottky diode is forward biased free electrons on n-side gain enough energy to flow into the metal causing forward current. Since the metal does not have any holes there is no charge storage, decreasing the recovery time. Therefore a Schottky diode can switch-off faster than an ordinary p-n junction diode. A Schottky diode has a relatively low forward voltage drop and reverse recovery losses. The leakage current is higher than a p-n junction diode. The maximum allowable voltage is about 100 V. Current ratings vary from about 1 to 300 A. They are mostly used in low voltage and high current dc power supplies. The operating frequency may be as high 100-300 kHz as the device is suitable for high frequency application. Schottky diode is also known as hot carrier diode.

General Purpose Diodes are available upto 5000V, 3500A. The rating of fast-recovery diodes can go upto 3000V, 1000A. The reverse recovery time varies between 0.1 and 5μsec. The fast recovery diodes are essential for high frequency switching of power converters. Schottky diodes have low-on-state voltage drop and very small
recovery time, typically a few nanoseconds. Hence turn-off time is very low for schottky diodes. The leakage current increases with the voltage rating and their ratings are limited to 100V, 300A. The diode turns on and begins to conduct when it is forward biased. When the anode voltage is greater than the cathode voltage diode conducts.

The forward voltage drop of a power diode is low typically 0.5V to 1.2V. If the cathode voltage is higher than its anode voltage then the diode is said to be reverse biased.

Power diodes of high current rating are available in
- Stud or stud-mounted type.
- Disk or press pack or Hockey-pack type.

In a stud mounted type, either the anode or the cathode could be the stud.

### COMPARISON BETWEEN DIFFERENT TYPES OF DIODES

<table>
<thead>
<tr>
<th>General Purpose Diodes</th>
<th>Fast Recovery Diodes</th>
<th>Schottky Diodes</th>
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<tbody>
<tr>
<td>Upto 5000V &amp; 3500A</td>
<td>Upto 3000V and 1000A</td>
<td>Upto 100V and 300A</td>
</tr>
<tr>
<td>Reverse recovery time – High</td>
<td>Reverse recovery time – Low</td>
<td>Reverse recovery time – Extremely low.</td>
</tr>
<tr>
<td>$t_r \approx 25\mu s$</td>
<td>$t_r = 0.1\mu s$ to $5\mu s$</td>
<td>$t_r = \text{a few nanoseconds}$</td>
</tr>
<tr>
<td>Turn off time – High</td>
<td>Turn off time – Low</td>
<td>Turn off time – Extremely low</td>
</tr>
<tr>
<td>Switching frequency – Low</td>
<td>Switching frequency – High</td>
<td>Switching frequency – Very high.</td>
</tr>
<tr>
<td>$V_F = 0.7V$ to $1.2V$</td>
<td>$V_F = 0.8V$ to $1.5V$</td>
<td>$V_F \approx 0.4V$ to $0.6V$</td>
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Natural or AC line commutated Thyristors are available with ratings upto 6000V, 3500A.

The turn-off time of high speed reverse blocking Thyristors have been improved substantially and now devices are available with $t_{OFF} = 10$ to $20\mu$sec for a 1200V, 2000A Thyristors.

RCT’s (reverse conducting Thyristors) and GATT’s (gate assisted turn-off Thyristors) are widely used for high speed switching especially in traction applications. An RCT can be considered as a thyristor with an inverse parallel diode. RCT’s are available up to 2500V, 1000A (& 400A in reverse conduction) with a switching time of 40μsec. GATT’s are available upto 1200V, 400A with a switching speed of 8μsec. LASCR’s which are available upto 6000V, 1500A with a switching speed of 200μsec to 400μsec are suitable for high voltage power systems especially in HVDC.

For low power AC applications, triac’s are widely used in all types of simple heat controls, light controls, AC motor controls, and AC switches. The characteristics of triac’s are similar to two SCR’s connected in inverse parallel and having only one gate terminal. The current flow through a triac can be controlled in either direction.

**GTO’s & SITH’s** are self turn-off Thyristors. GTO’s & SITH’s are turned ON by applying and short positive pulse to the gate and are turned off by applying short negative pulse to the gates. They do not require any commutation circuits.

GTO’s are very attractive for forced commutation of converters and are available upto 4000V, 3000A.
SITH’s with rating as high as 1200V and 300A are expected to be used in medium power converters with a frequency of several hundred KHz and beyond the frequency range of GTO.

An MCT (MOS controlled thyristor) can be turned ON by a small negative voltage pulse on the MOS gate (with respect to its anode) and turned OFF by a small positive voltage pulse. It is like a GTO, except that the turn off gain is very high. MCT’s are available up to 1000V and 100A.

High power bipolar transistors (high power BJT’s) are commonly used in power converters at a frequency below 10KHz and are effectively used in circuits with power ratings up to 1200V, 400A.

A high power BJT is normally operated as a switch in the common emitter configuration.

The forward voltage drop of a conducting transistor (in the ON state) is in the range of 0.5V to 1.5V across collector and emitter. That is $V_{CE} = 0.5V$ to $1.5V$ in the ON state.

**POWER TRANSISTORS**

Transistors which have high voltage and high current rating are called power transistors. Power transistors used as switching elements, are operated in saturation region resulting in a low - on state voltage drop. Switching speed of transistors are much higher than the thyristors, and they are extensively used in dc-dc and dc-ac converters with inverse parallel connected diodes to provide bi-directional current flow. However, voltage and current ratings of power transistor are much lower than the thyristors. Transistors are used in low to medium power applications. Transistors are current controlled device and to keep it in the conducting state, a continuous base current is required.

Power transistors are classified as follows

- Bi-Polar Junction Transistors (BJTs)
- Metal-Oxide Semi-Conductor Field Effect Transistors (MOSFETs)
- Insulated Gate Bi-Polar Transistors (IGBTs)
- Static Induction Transistors (SITs)

**BI-POLAR JUNCTION TRANSISTOR**

A Bi-Polar Junction Transistor is a 3 layer, 3 terminals device. The 3 terminals are base, emitter and collector. It has 2 junctions’ collector-base junction (CB) and emitter-base junction (EB). Transistors are of 2 types, NPN and PNP transistors.

The different configurations are common base, common collector and common emitter. Common emitter configuration is generally used in switching applications.
Transistors can be operated in 3 regions i.e., cut-off, active and saturation.

In the cut-off region transistor is OFF, both junctions (EB and CB) are reverse biased. In the cut-off state the transistor acts as an open switch between the collector and emitter.

In the active region, transistor acts as an amplifier (CB junction is reverse biased and EB junction is forward biased),

In saturation region the transistor acts as a closed switch and both the junctions CB and EB are forward biased.

SWITCHING CHARACTERISTICS

An important application of transistor is in switching circuits. When transistor is used as a switch it is operated either in cut-off state or in saturation state. When the transistor is driven into the cut-off state it operates in the non-conducting state. When the transistor is operated in saturation state it is in the conduction state.

Thus the non-conduction state is operation in the cut-off region while the conducting state is operation in the saturation region.

As the base voltage $V_B$ rises from 0 to $V_B$, the base current rises to $I_B$, but the collector current does not rise immediately. Collector current will begin to increase only when the base emitter junction is forward biased and $V_{BE} > 0.6V$. The collector current $I_C$ will gradually increase towards saturation level $I_{C_{sat}}$. The time required for the collector current to rise to 10% of its final value is called delay time $t_d$. The time taken by the collector current to rise from 10% to 90% of its final value is called rise time $t_r$. Turn on times is sum of $t_d$ and $t_r$, $t_{on} = t_d + t_r$.
The turn-on time depends on
- Transistor junction capacitances which prevent the transistors voltages from changing instantaneously.
- Time required for emitter current to diffuse across the base region into the collector region once the base emitter junction is forward biased. The turn on time $t_{on}$ ranges from 10 to 300 ns. Base current is normally more than the minimum required to saturate the transistor. As a result excess minority carrier charge is stored in the base region.

When the input voltage is reversed from $V_{B1}$ to $-V_{B2}$ the base current also abruptly changes but the collector current remains constant for a short time interval $t_s$ called the storage time.

The reverse base current helps to discharge the minority charge carries in the base region and to remove the excess stored charge form the base region. Once the excess stored charge is removed the base current begins to fall towards zero. The fall-time $t_f$ is the time taken for the collector current to fall from 90% to 10% of $I_{C(sat)}$. The turn off time $t_{off}$ is the sum of storage time and the fall time. $t_{off} = t_s + t_f$

Fig: Switching Times of Bipolar Junction Transistor
**DIAC**

A diac is a two terminal five layer semi-conductor bi-directional switching device. It can conduct in both directions. The device consists of two p-n-p-n sections in anti parallel as shown in figure. $T_1$ and $T_2$ are the two terminals of the device.

![Diac Structure](image1.png)

![Diac Symbol](image2.png)

Figure above shows the symbol of diac. Diac will conduct when the voltage applied across the device terminals $T_1$ & $T_2$ exceeds the break over voltage.

![Circuit Diagram 1](image3.png)

![Circuit Diagram 2](image4.png)

Figure 1.1 shows the circuit diagram with $T_1$ positive with respect to $T_2$. When the voltage across the device is less than the break over voltage $V_{b01}$, a very small amount of current called leakage current flows through the device. During this period the device is in non-conducting or blocking mode. But once the voltage across the diac exceeds the break over voltage $V_{b01}$, the diac turns on and begins to conduct. Once it starts conducting the current through diac becomes large and the device current has to be limited by connecting an external load resistance $R_L$, at the same time the voltage across the diac decreases in the conduction state. This explain the forward characteristics.

Figure 1.2 shows the circuit diagram with $T_2$ positive with respect to $T_1$. The reverse characteristics obtained by varying the supply voltage are identical with the forward characteristic as the device construction is symmetrical in both the directions. In both the cases the diac exhibits negative resistance switching characteristic during conduction. i.e., current flowing through the device increases whereas the voltage across it decreases.
Figure below shows forward and reverse characteristics of a diac. Diac is mainly used for triggering triacs.

**Diac Characteristics**

**TRIAC**

A triac is a three terminal bi-directional switching thyristor device. It can conduct in both directions when it is triggered into the conduction state. The triac is equivalent to two SCRs connected in anti-parallel with a common gate. Figure below shows the triac structure. It consists of three terminals viz., $MT_2$, $MT_1$ and gate G.

![Triac Structure](image)

The gate terminal G is near the $MT_1$ terminal. Figure above shows the triac symbol. $MT_1$ is the reference terminal to obtain the characteristics of the triac. A triac can be operated in four different modes depending upon the polarity of the voltage on the terminal $MT_2$ with respect to $MT_1$ and based on the gate current polarity.

The characteristics of a triac is similar to that of an SCR, both in blocking and conducting states. A SCR can conduct in only one direction whereas triac can conduct in both directions.
TRIGGERING MODES OF TRIAC

MODE 1: $MT_2$ positive, Positive gate current  \( (I^+ \text{ mode of operation}) \)

When $MT_2$ and gate current are positive with respect to $MT_1$, the gate current flows through $P_2-N_2$ junction as shown in figure below. The junction $P_1-N_1$ and $P_2-N_2$ are forward biased but junction $N_1-P_2$ is reverse biased. When sufficient number of charge carriers are injected in $P_2$ layer by the gate current the junction $N_1-P_2$ breakdown and triac starts conducting through $P_1N_1P_2N_2$ layers. Once triac starts conducting the current increases and its V-I characteristics is similar to that of thyristor. Triac in this mode operates in the first-quadrant.

![Mode 1 Diagram](image1)

MODE 2: $MT_2$ positive, Negative gate current  \( (I^- \text{ mode of operation}) \)

When $MT_2$ is positive and gate $G$ is negative with respect to $MT_1$ the gate current flows through $P_2-N_3$ junction as shown in figure above. The junction $P_1-N_1$ and $P_2-N_3$ are forward biased but junction $N_1-P_2$ is reverse biased. Hence, the triac initially starts conducting through $P_1N_1P_2N_3$ layers. As a result the potential of layer between $P_2-N_3$ rises towards the potential of $MT_2$. Thus, a potential gradient exists across the layer $P_2$ with left hand region at a higher potential than the right hand region. This results in a current flow in $P_2$ layer from left to right, forward biasing the $P_2N_2$ junction. Now the right hand portion $P_1-N_1 - P_2-N_2$ starts conducting. The device operates in first quadrant.

![Mode 2 Diagram](image2)
When compared to Mode 1, triac with $MT_2$ positive and negative gate current is less sensitive and therefore requires higher gate current for triggering.

**MODE 3 : $MT_2$ negative, Positive gate current (III$^+$ mode of operation)**

When $MT_2$ is negative and gate is positive with respect to $MT_1$ junction $P_2N_2$ is forward biased and junction $P_1N_1$ is reverse biased. $N_2$ layer injects electrons into $P_2$ layer as shown by arrows in figure below. This causes an increase in current flow through junction $P_2-N_1$. Resulting in breakdown of reverse biased junction $N_1-P_1$. Now the device conducts through layers $P_2N_1P_1N_4$ and the current starts increasing, which is limited by an external load.

![Diagram](image1)

The device operates in third quadrant in this mode. Triac in this mode is less sensitive and requires higher gate current for triggering.

**MODE 4 : $MT_2$ negative, Negative gate current (III$^-$ mode of operation)**

In this mode both $MT_2$ and gate $G$ are negative with respect to $MT_1$, the gate current flows through $P_2N_3$ junction as shown in figure above. Layer $N_3$ injects electrons as shown by arrows into $P_2$ layer. This results in increase in current flow across $P_1N_1$ and the device will turn ON due to increased current in layer $N_1$. The current flows
through layers $P_2 N_1 P_1 N_4$. Triac is more sensitive in this mode compared to turn ON with positive gate current. (Mode 3).

Triac sensitivity is greatest in the first quadrant when turned ON with positive gate current and also in third quadrant when turned ON with negative gate current. when $MT_2$ is positive with respect to $MT_1$ it is recommended to turn on the triac by a positive gate current. When $MT_2$ is negative with respect to $MT_1$ it is recommended to turn on the triac by negative gate current. Therefore Mode 1 and Mode 4 are the preferred modes of operation of a triac ($I^+$ mode and $III^-$ mode of operation are normally used).

TRIAC CHARACTERISTICS

Figure below shows the circuit to obtain the characteristics of a triac. To obtain the characteristics in the third quadrant the supply to gate and between $MT_2$ and $MT_1$ are reversed.

Figure below shows the V-I Characteristics of a triac. Triac is a bidirectional switching device. Hence its characteristics are identical in the first and third quadrant. When gate current is increased the break over voltage decreases.

Fig.: Triac Characteristic
Triac is widely used to control the speed of single phase induction motors. It is also used in domestic lamp dimmers and heat control circuits, and full wave AC voltage controllers.

**POWER MOSFET**

Power MOSFET is a metal oxide semiconductor field effect transistor. It is a voltage controlled device requiring a small input gate voltage. It has high input impedance. MOSFET is operated in two states viz., ON STATE and OFF STATE. Switching speed of MOSFET is very high. Switching time is of the order of nanoseconds.

MOSFETs are of two types
- Depletion MOSFETs
- Enhancement MOSFETs.

MOSFET is a three terminal device. The three terminals are gate (G), drain (D) and source (S).

**DEPLETION MOSFET**

Depletion type MOSFET can be either a n-channel or p-channel depletion type MOSFET. A depletion type n-channel MOSFET consists of a p-type silicon substrate with two highly doped n⁺ silicon for low resistance connections. A n-channel is diffused between drain and source. Figure below shows a n-channel depletion type MOSFET. Gate is isolated from the channel by a thin silicon dioxide layer.

Gate to source voltage (V\(_{\text{GS}}\)) can be either positive or negative. If V\(_{\text{GS}}\) is negative, electrons present in the n-channel are repelled leaving positive ions. This creates a depletion.
Figure above shows a p-channel depletion type MOSFET. A P-channel depletion type MOSFET consists of a n-type substrate into which highly doped p-regions and a P-channel are diffused. The two P⁺ regions act as drain and source P-channel operation is same except that the polarities of voltages are opposite to that of n-channel.

ENHANCEMENT MOSFET

Enhancement type MOSFET has no physical channel. Enhancement type MOSFET can be either a n-channel or p-channel enhancement type MOSFET.

Figure above shows a n-channel enhancement type MOSFET. The P-substrate extends upto the silicon dioxide layer. The two highly doped n regions act as drain and source.

When gate is positive (V_{GS}) free electrons are attracted from P-substrate and they collect near the oxide layer. When gate to source voltage, V_{GS} becomes greater than or equal to a value called threshold voltage (V_T). Sufficient numbers of electrons are accumulated to form a virtual n-channel and current flows from drain to source.

Figure below shows a p-channel enhancement type of MOSFET. The n-substrate extends upto the silicon dioxide layer. The two highly doped P regions act as drain and source. For p-channel the polarities of voltages are opposite to that of n-channel.
CHARACTERISTICS OF MOSFET

Depletion MOSFET

Figure below shows n-channel depletion type MOSFET with gate positive with respect to source. \( I_D, V_{DS} \) and \( V_{GS} \) are drain current, drain source voltage and gate-source voltage. A plot of variation of \( I_D \) with \( V_{DS} \) for a given value of \( V_{GS} \) gives the Drain characteristics or Output characteristics.

\[ V_{GS} \quad I_D \quad V_{DS} \quad R_D \quad V_{DD} \]

Fig: n-channel Depletion MOSFET

n-channel Depletion type MOSFET

\( V_{GS} \) & \( V_{DS} \) are positive. \( I_D \) is positive for n channel MOSFET. \( V_{GS} \) is negative for depletion mode. \( V_{GS} \) is positive for enhancement mode.

Figure below shows the drain characteristic. MOSFET can be operated in three regions

- Cut-off region,
- Saturation region (pinch-off region) and
- Linear region.

In the linear region \( I_D \) varies linearly with \( V_{DS} \) i.e., increases with increase in \( V_{DS} \).

Power MOSFETs are operated in the linear region for switching actions. In saturation region \( I_D \) almost remains constant for any increase in \( V_{DS} \).
Figure below shows the transfer characteristic. Transfer characteristic gives the variation of $I_D$ with $V_{GS}$ for a given value of $V_{DS}$. $I_{DSS}$ is the drain current with shorted gate. As curve extends on both sides $V_{GS}$ can be negative as well as positive.

**Enhancement MOSFET**

$V_{GS}$ is positive for a n-channel enhancement MOSFET. $V_{DS}$ & $I_D$ are also positive for n-channel enhancement MOSFET.
Figure above shows circuit to obtain characteristic of n channel enhancement type MOSFET. Figure below shows the drain characteristic. Drain characteristic gives the variation of $I_D$ with $V_{DS}$ for a given value of $V_{GS}$.

\[ V_T = V_{GS(TH)} = \text{Gate Source Threshold Voltage} \]

**Fig.: Transfer Characteristic**

Figure below shows the transfer characteristic which gives the variation of $I_D$ with $V_{GS}$ for a given value of $V_{DS}$.

**Fig.: Drain Characteristic**

**MOSFET PARAMETERS**

The parameters of MOSFET can be obtained from the graph as follows.

Mutual Transconductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ / $V_{DS} = \text{Constant}$ .

Output or Drain Resistance $R_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} / V_{GS} = \text{Constant}$ .

Amplification factor $\mu = R_{ds} \times g_m$
Power MOSFETs are generally of enhancement type. Power MOSFETs are used in switched mode power supplies.

Power MOSFET’s are used in high speed power converters and are available at a relatively low power rating in the range of 1000V, 50A at a frequency range of several tens of KHz \( f_{\text{max}} = 100\text{KHz} \).

**SWITCHING CHARACTERISTICS OF MOSFET**

Power MOSFETs are often used as switching devices. The switching characteristic of a power MOSFET depends on the capacitances between gate to source \( C_{GS} \), gate to drain \( C_{GD} \) and drain to source \( C_{GS} \). It also depends on the impedance of the gate drive circuit. During turn-on there is a turn-on delay \( t_{d(on)} \), which is the time required for the input capacitance \( C_{GS} \) to charge to threshold voltage level \( V_T \). During the rise time \( t_r \), \( C_{GS} \) charges to full gate voltage \( V_{GSP} \) and the device operate in the linear region (ON state). During rise time \( t_r \), drain current \( I_D \) rises from zero to full on state current \( I_D \).

- Total turn-on time, \( t_{on} = t_{d(on)} + t_r \)

MOSFET can be turned off by discharging capacitance \( C_{GS} \). \( t_{d(off)} \) is the turn-off delay time required for input capacitance \( C_{GS} \) to discharge from \( V_1 \) to \( V_{GSP} \). Fall time \( t_f \) is the time required for input capacitance to discharge from \( V_{GSP} \) to threshold voltage \( V_T \). During fall time \( t_f \), drain current falls from \( I_D \) to zero. Figure below shows the switching waveforms of power MOSFET.

![Switching waveforms of power MOSFET](attachment:image.png)
INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

IGBT is a voltage controlled device. It has high input impedance like a MOSFET and low on-state conduction losses like a BJT.

Figure below shows the basic silicon cross-section of an IGBT. Its construction is same as power MOSFET except that \( n^+ \) layer at the drain in a power MOSFET is replaced by \( p^+ \) substrate called collector.

![IGBT Cross-Section and Symbol](image)

**Fig.: Insulated Gate Bipolar Transistor**

IGBT has three terminals gate (G), collector (C) and emitter (E). With collector and gate voltage positive with respect to emitter the device is in forward blocking mode. When gate to emitter voltage becomes greater than the threshold voltage of IGBT, a \( n^- \) channel is formed in the \( P^- \) region. Now device is in forward conducting state. In this state \( p^+ \) substrate injects holes into the epitaxial \( n^- \) layer. Increase in collector to emitter voltage will result in increase of injected hole concentration and finally a forward current is established.

CHARACTERISTIC OF IGBT

Figure below shows circuit diagram to obtain the characteristic of an IGBT. An output characteristic is a plot of collector current \( I_C \) versus collector to emitter voltage \( V_{CE} \) for given values of gate to emitter voltage \( V_{GE} \).
A plot of collector current $I_C$ versus gate-emitter voltage $V_{GE}$ for a given value of $V_{CE}$ gives the transfer characteristic. Figure below shows the transfer characteristic.

**Note**

Controlling parameter is the gate-emitter voltage $V_{GE}$ in IGBT. If $V_{GE}$ is less than the threshold voltage $V_T$ then IGBT is in OFF state. If $V_{GE}$ is greater than the threshold voltage $V_T$ then the IGBT is in ON state.

IGBTs are used in medium power applications such as ac and dc motor drives, power supplies and solid state relays.
SWITCHING CHARACTERISTIC OF IGBT

Figure below shows the switching characteristic of an IGBT. Turn-on time consists of delay time $t_{(on)}$ and rise time $t_r$.

![Switching Characteristics Diagram]

The turn-on delay time is the time required by the leakage current $I_{CE}$ to rise to $0.1 I_C$, where $I_C$ is the final value of collector current. Rise time is the time required for collector current to rise from $0.1 I_C$ to its final value $I_C$. After turn-on collector-emitter voltage $V_{CE}$ will be very small during the steady state conduction of the device.

The turn-off time consists of delay off time $t_{(off)}$ and fall time $t_f$. Off time delay is the time during which collector current falls from $I_C$ to $0.9 I_C$ and $V_{GE}$ falls to threshold voltage $V_{GET}$. During the fall time $t_f$ the collector current falls from $0.90 I_C$ to $0.1 I_C$. During the turn-off time interval collector-emitter voltage rises to its final value $V_{CE}$.

IGBT’s are voltage controlled power transistor. They are faster than BJT’s, but still not quite as fast as MOSFET’s. the IGBT’s offer for superior drive and output characteristics when compared to BJT’s. IGBT’s are suitable for high voltage, high current and frequencies up to 20KHz. IGBT’s are available up to 1400V, 600A and 1200V, 1000A.
IGBT APPLICATIONS
Medium power applications like DC and AC motor drives, medium power supplies, solid state relays and contractors, general purpose inverters, UPS, welder equipments, servo controls, robotics, cutting tools, induction heating

TYPICAL RATINGS OF IGBT
Voltage rating = 1400V. Current rating = 600A. Maximum operating frequency = 20KHz. Switching time \( t_{ON} \approx t_{OFF} \). On state resistance = 600m\( \Omega \) = 60x10^{-3} \Omega.

POWER MOSFET RATINGS
Voltage rating = 500V. Current rating = 50A. Maximum operating frequency = 100KHz. Switching time = 0.6\( \mu \)s to 1\( \mu \)s \( t_{ON} \approx t_{OFF} \). On state resistance \( R_{D(ON)} \) = 0.4m\( \Omega \) to 0.6m\( \Omega \).

A MOSFET/IGBT SWITCH

MOSFET / IGBT can be used as a switch in the circuit shown above. If a n-channel enhancement MOSFET is used then the input pulse is \( V_{GS} \) which is the pulse applied between gate and source, which is a positive going voltage pulse.

IGBT’s
Minority carrier devices, superior conduction characteristics, ease of drive, wide SOA, peak current capability and ruggedness. Generally the switching speed of an IGBT is inferior to that of a power MOSFET.

POWER MOSFET’s (MAJORITY CARRIER DEVICES)
Higher switching speed, peak current capability, ease of drive, wide SOA, avalanche and \( \frac{d_i}{d_t} \) capability have made power MOSFET is the ideal choice in new power electronic circuit designs.
IGBT (INSULATED GATE BIPOLAR TRANSISTORS) FEATURES
IGBT combines the advantages of BJT’s and MOSFET’s. Features of IGBT are
- IGBT has high input impedance like MOSFET’s.
- Low ON state conduction power losses like BJT’s.
- There is no secondary breakdown problem like BJT’s.
- By chip design and structure design, the equivalent drain to source resistance $R_{DS}$ is controlled to behave like that of BJT.

DATA SHEET DETAILS OF THE IGBT MODULE CM400HA-24H
High power switching device by Mitsubishi Semiconductors Company
$I_C = 400A$, $V_{CES} = 1200V$.

APPLICATIONS OF IGBT CM400HA-24H
AC and DC motor controls, general purpose inverters, UPS, welders, servo controls, numeric control, robotics, cutting tools, induction heating.

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CES}$ Collector-Emitter (G-E short) voltage</td>
<td>1200V</td>
</tr>
<tr>
<td>$V_{GES}$ Gate-Emitter (C-E short) voltage</td>
<td>±20V</td>
</tr>
<tr>
<td>$I_C$ Collector Current (steady / average current)</td>
<td>400A at $T_C = 25^0C$</td>
</tr>
<tr>
<td>$I_{CM}$ Pulsed Collector Current</td>
<td>800A</td>
</tr>
<tr>
<td>$I_E$ Emitter Current</td>
<td>400A at $T_C = 25^0C$</td>
</tr>
<tr>
<td>$I_{EM}$ Maximum Pulsed Emitter Current</td>
<td>800A</td>
</tr>
<tr>
<td>$P_{C(max)}$ Maximum Collector Power Dissipation</td>
<td>2800W at $T_C = 25^0C$</td>
</tr>
<tr>
<td>$T_{storage}$ Maximum Storage Temperature</td>
<td>$-40^0c$ to $125^0c$</td>
</tr>
<tr>
<td>$T_J$ Junction Temperature</td>
<td>$-40^0c$ to $150^0c$</td>
</tr>
<tr>
<td>Weight Typical Value</td>
<td>400gm (0.4Kg)</td>
</tr>
</tbody>
</table>

Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GE(th)}$ = $V_{TH}$ = Gate – Emitter Threshold Voltage.</td>
<td>$V_{GE(th)}$ = 6V (Typ)</td>
</tr>
<tr>
<td>$V_{GE(th)}$ = 4.5V (min) to 7.5V maximum at $I_C = 40mA$ and $V_{CE} = 10V$ .</td>
<td></td>
</tr>
<tr>
<td>$I_{CES}$ Collector cut-off current = $2mA$ (maximum) at $V_{CE} = V_{CES}, V_{GE} = 0$</td>
<td></td>
</tr>
<tr>
<td>$I_{GES}$ Gate leakage current = $0.5\mu A$ (maximum) at $V_{GE} = V_{GES}, V_{CE} = 0$</td>
<td></td>
</tr>
<tr>
<td>$V_{CE(sat)}$ Collector-Emitter saturation voltage ($T_J = 25^0C, I_C = 400A, V_{GE} = 15V$ )</td>
<td>2.5V (typical), 3.5V (maximum)</td>
</tr>
<tr>
<td>$t_{d(on)}$ Turn ON delay time 300nsec (maximum) at $V_{CC} = 600V, I_C = 400A$ .</td>
<td></td>
</tr>
<tr>
<td>$t_r$ Turn ON rise time 500nsec (maximum), at $V_{GE1} = V_{GE2} = 15V$ .</td>
<td></td>
</tr>
<tr>
<td>$t_{ON} = 800\mu s (max) = (t_d + t_r)$</td>
<td></td>
</tr>
<tr>
<td>$t_{d(OFF)}$ Turn off delay time = 350nsec.</td>
<td></td>
</tr>
<tr>
<td>$t_f$ Turn off fall time = 350nsec.</td>
<td></td>
</tr>
</tbody>
</table>
\[ t_{OFF} = t_{d(OFF)} + t_f = 700\text{nsec (maximum)} \]

- \( t_{rr} \)  Reverse recovery time 250nsec.
- \( Q_{rr} \)  Reverse recovery charge = 2.97\( \mu \text{C} \) (typical).

**CHARACTERISTICS OF THE EMITTER TO COLLECTOR FWD CM 400HA-24H IGBT CHARACTERISTICS**

**Fig: Output Collector Characteristics**

**Fig: Transfer Characteristics**
POWER SEMICONDUCTOR DEVICES, THEIR SYMBOLS AND CHARACTERISTICS

- **Diode**
  - Symbol: A → K, I_D, V_AK
  - Characteristics: I_D ↑ → V_AK

- **Thyrister**
  - Symbol: A → G → K, I_A, V_AK
  - Characteristics: Gate triggered

- **SITH**
  - Symbol: A → G → K

- **GTO**
  - Symbol: A → G → K, I_A, V_AK
  - Characteristics: Gate triggered

- **MCT**
  - Symbol: A → G

- **LASCR**
  - Symbol: A → G → K, I_A, V_AK
  - Characteristics: Gate triggered

- **NPN BJT**
  - Symbol: B → E → C
  - Characteristics: I_A, I_E, I_C

- **IGBT**
  - Symbol: G → C
  - Characteristics: V_GS, V_CE, V_T

- **N-Channel MOSFET**
  - Symbol: G → D → S
  - Characteristics: V_GS, V_DS

- **SIT**
  - Symbol: G → D → S
  - Characteristics: V_GS, V_ES
CONTROL CHARACTERISTICS OF POWER DEVICES

The power semiconductor devices can be operated as switches by applying control signals to the gate terminal of Thyristors (and to the base of bi-polar transistor). The required output is obtained by varying the conduction time of these switching devices. Figure below shows the output voltages and control characteristics of commonly used power switching devices. Once a thyristor is in a conduction mode, the gate signal of either positive or negative magnitude has no effect. When a power semiconductor device is in a normal conduction mode, there is a small voltage drop across the device. In the output voltage waveforms shown, these voltage drops are considered negligible.
The power semiconductor switching devices can be classified on the basis of
- Uncontrolled turn on and turn off (e.g.: diode).
- Controlled turn on and uncontrolled turn off (e.g. SCR)
- Controlled turn on and off characteristics (e.g. BJT, MOSFET, GTO, SITH, IGBT, SIT, MCT).
- Continuous gate signal requirement (e.g. BJT, MOSFET, IGBT, SIT).
- Pulse gate requirement (e.g. SCR, GTO, MCT).
- Bipolar voltage withstanding capability (e.g. SCR, GTO).
- Unipolar voltage withstanding capability (e.g. BJT, MOSFET, GTO, IGBT, MCT).
- Bidirectional current capability (e.g.: Triac, RCT).
- Unidirectional current capability (e.g. SCR, GTO, BJT, MOSFET, MCT, IGBT, SITH, SIT & Diode).
THYRISTORISED POWER CONTROLLERS

Block diagram given below, shows the system employing a thyristorised power controller. The main power flow between the input power source and the load is shown by solid lines.

Thyristorised power controllers are widely used in the industry. Old/conventional controllers including magnetic amplifiers, mercury arc rectifiers, thyratrons, ignitrons, rotating amplifiers, resistance controllers have been replaced by thyristorised power controllers in almost all the applications.

A typical block diagram of a thyristorised power converter is shown in the above figure.

The thyristor power converter converts the available power from the source into a suitable form to run the load or the equipment. For example the load may be a DC motor drive which requires DC voltage for its operation. The available power supply is AC power supply as is often the case. The thyristor power converter used in this case is a AC to DC power converter which converts the input AC power into DC output voltage to feed to the DC motor. Very often a measuring unit or an instrumentation unit is used so as to measure and monitor the output parameters like the output voltage, the load current, the speed of the motor or the temperature etc. The measuring unit will be provided with meters and display devices so that the output parameters can be seen and noted. The control unit is employed to control the output of the thyristorised power converter so as to adjust the output voltage / current to the desired value to obtain optimum performance of the load or equipment. The signal from the control unit is used to adjust the phase angle / trigger angle of the Thyristors in the power controller so as to vary the output voltage to the desired value.

SOME IMPORTANT APPLICATIONS OF THYRISTORISED POWER CONTROLLERS

- Control of AC and DC motor drives in rolling mills, paper and textile mills, traction vehicles, mine winders, cranes, excavators, rotary kilns, ventilation fans, compression etc.
- Uninterruptible and stand by power supplies for critical loads such as computers, special high tech power supplies for aircraft and space applications.
- Power control in metallurgical and chemical processes using arc welding, induction heating, melting, resistance heating, arc melting, electrolysis, etc.
- Static power compensators, transformer tap changers and static contactors for industrial power systems.
• Power conversion at the terminals of a HVDC transmission systems.
• High voltage supplies for electrostatic precipitators and x-ray generators.
• Illumination/light control for lighting in stages, theaters, homes and studios.
• Solid state power controllers for home/domestic appliances.

ADVANTAGES OF THYRISTORISED POWER CONTROLLERS
• High efficiency due to low losses in the Thyristors.
• Long life and reduced/minimal maintenance due to the absence of mechanical wear.
• Control equipments using Thyristors are compact in size.
• Easy and flexibility in operation due to digital controls.
• Faster dynamic response compared to the electro mechanical converters.
• Lower acoustic noise when compared to electro magnetic controllers, relays and contactors.

DISADVANTAGES OF THYRISTORISED POWER CONTROLLERS
• All the thyristorised power controllers generate harmonics (unwanted frequency components) due to the switching ON and OFF of the thyristors. These harmonics adversely affect the performance of the load connected to them. For example when the load are motors, there are additional power losses (harmonic power loss) torque harmonics, and increase in acoustic noise.
• The generated harmonics are injected into the supply lines and thus adversely affect the other loads/equipments connected to the supply lines.
• In some applications example: traction, there is interference with the commutation circuits due to the power supply line harmonics and due to electromagnetic radiation.
• The thyristorised AC to DC converters and AC to AC converters can operate at low power factor under some conditions.
• Special steps are then taken for correcting the line supply power factor (by installing PF improvement apparatus).
• The thyristorised power controllers have no short time over loading capacity and therefore they must be rated for maximum loading conditions. This leads to an increase in the cost of the equipment.
• Special protection circuits must be employed in thyristorised power controllers in order to protect and safeguard the expensive thyristor devices. This again adds to the system cost.

TYPES OF POWER CONVERTERS or THYRISTORISED POWER CONTROLLERS
For the control of electric power supplied to the load or the equipment/machinery or for power conditioning the conversion of electric power from one form to other is necessary and the switching characteristic of power semiconductor devices (Thyristors) facilitate these conversions.

The thyristorised power converters are referred to as the static power converters and they perform the function of power conversion by converting the available input power supply into output power of desired form.

The different types of thyristor power converters are
• Diode rectifiers (uncontrolled rectifiers).
- Line commutated converters or AC to DC converters (controlled rectifiers)
- AC voltage (RMS voltage) controllers (AC to AC converters).
- Cyclo converters (AC to AC converters at low output frequency).
- DC choppers (DC to DC converters).
- Inverters (DC to AC converters).

**LINE COMMUTATED CONVERTERS (AC TO DC CONVERTERS)**

These are AC to DC converters. The line commutated converters are AC to DC power converters. These are also referred to as controlled rectifiers. The line commutated converters (controlled rectifiers) are used to convert a fixed voltage, fixed frequency AC power supply to obtain a variable DC output voltage. They use natural or AC line commutation of the Thyristors.

**Fig:** A Single Phase Full Wave Uncontrolled Rectifier Circuit (Diode Full Wave Rectifier) using a Center Tapped Transformer
Fig: A Single Phase Full Wave Controlled Rectifier Circuit (using SCRs) using a Center Tapped Transformer

Different types of line commutated AC to DC converters circuits are
- Diode rectifiers – Uncontrolled Rectifiers
- Controlled rectifiers using SCR’s.
  - Single phase controlled rectifier.
  - Three phase controlled rectifiers.

Applications Of Line Commutated Converters
AC to DC power converters are widely used in
- Speed control of DC motor in DC drives.
- UPS.
- HVDC transmission.
- Battery Chargers.

AC VOLTAGE REGULATORS OR RMS VOLTAGE CONTROLLERS (AC TO AC CONVERTERS)

The AC voltage controllers convert the constant frequency, fixed voltage AC supply into variable AC voltage at the same frequency using line commutation.
AC regulators (RMS voltage controllers) are mainly used for
- Speed control of AC motor.
- Speed control of fans (domestic and industrial fans).
- AC pumps.
CYCLO CONVERTERS (AC TO AC CONVERTERS WITH LOW OUTPUT FREQUENCY)

The cyclo converters convert power from a fixed voltage fixed frequency AC supply to a variable frequency and variable AC voltage at the output.

The cyclo converters generally produce output AC voltage at a lower output frequency. That is output frequency of the AC output is less than input AC supply frequency.

Applications of cyclo converters are traction vehicles and gearless rotary kilns.

CHOPPERS (DC TO DC CONVERTERS)

The choppers are power circuits which obtain power from a fixed voltage DC supply and convert it into a variable DC voltage. They are also called as DC choppers or DC to DC converters. Choppers employ forced commutation to turn off the Thyristors.
DC choppers are further classified into several types depending on the direction of power flow and the type of commutation. DC choppers are widely used in

- Speed control of DC motors from a DC supply.
- DC drives for sub-urban traction.
- Switching power supplies.

![DC Chopper Circuit](image)

**Fig: A DC Chopper Circuit (DC-DC Converter) using IGBT**

**INVERTERS (DC TO AC CONVERTERS)**

The inverters are used for converting DC power from a fixed voltage DC supply into an AC output voltage of variable frequency and fixed or variable output AC voltage. The inverters also employ force commutation method to turn off the Thyristors.

**Application of inverters** are in

- Industrial AC drives using induction and synchronous motors.
- Uninterrupted power supplies (UPS system) used for computers, computer labs.
DESIGN OF POWER ELECTRONICS CIRCUITS

The design and study of power electronic circuits involve
- Design and study of power circuits using Thyristors, Diodes, BJT’s or MOSFETS.
- Design and study of control circuits.
- Design and study of logic and gating circuits and associated digital circuits.
- Design and study of protection devices and circuits for the protection of thyristor power devices in power electronic circuits.

The power electronic circuits can be classified into six types
- Diode rectifiers (uncontrolled rectifiers)
- AC to DC converters (Controlled rectifiers)
- AC to AC converters (AC voltage controllers)
- DC to DC converters (DC choppers)
- DC to AC converters (Inverters)
- Static Switches (Thyristorized contactors)

PERIPHERAL EFFECTS

The power converter operations are based mainly on the switching of power semiconductor devices and as a result the power converters introduce current and voltage harmonics (unwanted AC signal components) into the supply system and on the output of the converters.

These induced harmonics can cause problems of distortion of the output voltage, harmonic generation into the supply system, and interference with the communication and signaling circuits. It is normally necessary to introduce filters on the input side and output side of a power converter system so as to reduce the harmonic level to an acceptable magnitude. The figure below shows the block diagram of a generalized power converter with filters added. The application of power electronics to supply the sensitive electronic loads poses a challenge on the power quality issues and raises the problems and concerns to be resolved by the researchers. The input and output quantities of power converters
could be either AC or DC. Factors such as total harmonic distortion (THD), displacement factor or harmonic factor (HF), and input power factor (IPF), are measures of the quality of the waveforms. To determine these factors it is required to find the harmonic content of the waveforms. To evaluate the performance of a converter, the input and output voltages/currents of a converter are expressed in Fourier series. The quality of a power converter is judged by the quality of its voltage and current waveforms.

![A General Power Converter System](image)

The control strategy for the power converters plays an important part on the harmonic generation and the output waveform distortion and can be aimed to minimize or reduce these problems. The power converters can cause radio frequency interference due to electromagnetic radiation and the gating circuits may generate erroneous signals. This interference can be avoided by proper grounding and shielding.
POWER TRANSISTORS

Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used as switching devices and are operated in the saturation region resulting in low on-state voltage drop. They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present. The switching speed of modern transistors is much higher than that of thyristors and are used extensively in dc-dc and dc-ac converters. However their voltage and current ratings are lower than those of thyristors and are therefore used in low to medium power applications.

Power transistors are classified as follows
- Bipolar junction transistors (BJTs)
- Metal-oxide semiconductor filed-effect transistors (MOSFETs)
- Static Induction transistors (SITs)
- Insulated-gate bipolar transistors (IGBTs)

BIPOLAR JUNCTION TRANSISTORS

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power BJT must have substantially different structure than its small signal equivalent. The modified structure leads to significant differences in the I-V characteristics and switching behavior between power transistors and its logic level counterpart.

POWER TRANSISTOR STRUCTURE

If we recall the structure of conventional transistor we see a thin p-layer is sandwiched between two n-layers or vice versa to form a three terminal device with the terminals named as Emitter, Base and Collector.

The structure of a power transistor is as shown below

Fig. 1: Structure of Power Transistor
The difference in the two structures is obvious.

A power transistor is a vertically oriented four layer structure of alternating p-type and n-type. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing. This also minimizes on-state resistance and thus power dissipation in the transistor.

The doping of emitter layer and collector layer is quite large typically $10^{19}$ cm$^{-3}$. A special layer called the collector drift region (n') has a light doping level of $10^{14}$.

The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

Practical power transistors have their emitters and bases interleaved as narrow fingers as shown. The purpose of this arrangement is to reduce the effects of current crowding. This multiple emitter layout also reduces parasitic ohmic resistance in the base current path which reduces power dissipation in the transistor.

![Fig. 2](image)

**STEADY STATE CHARACTERISTICS**

Figure 3(a) shows the circuit to obtain the steady state characteristics. Fig 3(b) shows the input characteristics of the transistor which is a plot of $I_B$ versus $V_{BE}$. Fig 3(c) shows the output characteristics of the transistor which is a plot $I_C$ versus $V_{CE}$. The characteristics shown are that for a signal level transistor.

The power transistor has steady state characteristics almost similar to signal level transistors except that the V-I characteristics has a region of quasi saturation as shown by figure 4.
Fig. 3: Characteristics of NPN Transistors
Fig. 4: Characteristics of NPN Power Transistors

There are four regions clearly shown: Cutoff region, Active region, quasi saturation and hard saturation. The cutoff region is the area where base current is almost zero. Hence no collector current flows and transistor is off. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on. Hence collector current flows depending upon the load. The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cutoff and saturation. The $BV_{SUS}$ is the maximum collector to emitter voltage that can be sustained when BJT is carrying substantial collector current. The $BV_{CEO}$ is the maximum collector to emitter breakdown voltage that can be sustained when base current is zero and $BV_{CBO}$ is the collector base breakdown voltage when the emitter is open circuited.

The primary breakdown shown takes place because of avalanche breakdown of collector base junction. Large power dissipation normally leads to primary breakdown.

The second breakdown shown is due to localized thermal runaway. This is explained in detail later.
TRANSFER CHARACTERISTICS

\[ I_E = I_C + I_B \]
\[ \beta = h_{ie} = \frac{I_C}{I_B} \]
\[ I_C = \beta I_B + I_{CEO} \]
\[ \alpha = \frac{\beta}{\beta + 1} \]
\[ \beta = \frac{\alpha}{1 - \alpha} \]

TRANSISTOR AS A SWITCH

The transistor is used as a switch therefore it is used only between saturation and cutoff. From fig. 5 we can write the following equations

![Fig. 6: Transistor Switch](image)
\begin{align*}
I_B &= \frac{V_B - V_{BE}}{R_B} \\
V_C &= V_{CE} = V_{CC} - I_C R_C \\
V_C &= V_{CC} - \beta \frac{R_C (V_B - V_{BE})}{R_B} \\
V_{CE} &= V_{CB} + V_{BE} \\
V_{CB} &= V_{CE} - V_{BE} \quad \text{...(1)}
\end{align*}

Equation (1) shows that as long as \( V_{CE} > V_{BE} \) the CBJ is reverse biased and transistor is in active region. The maximum collector current in the active region, which can be obtained by setting \( V_{CB} = 0 \) and \( V_{BE} = V_{CE} \) is given as

\[ I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} \quad \therefore \quad I_{BM} = \frac{I_{CM}}{\beta_f} \]

If the base current is increased above \( I_{BM} \), \( V_{BE} \) increases, the collector current increases and \( V_{CE} \) falls below \( V_{BE} \). This continues until the CBJ is forward biased with \( V_{BC} \) of about 0.4 to 0.5V, the transistor than goes into saturation. The transistor saturation may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In saturation, the collector current remains almost constant. If the collector emitter voltage is \( V_{CE(sat)} \) the collector current is

\[ I_{CS} = \frac{V_{CC} - V_{CESAT}}{R_C} \]

\[ I_{BS} = \frac{I_{CS}}{\beta} \]

Normally the circuit is designed so that \( I_B \) is higher that \( I_{BS} \). The ratio of \( I_B \) to \( I_{BS} \) is called to overdrive factor ODF.

\[ ODF = \frac{I_B}{I_{BS}} \]

The ratio of \( I_{CS} \) to \( I_B \) is called as forced \( \beta \).

\[ \beta_{forced} = \frac{I_{CS}}{I_B} \]

The total power loss in the two functions is

\[ P_I = V_{BE} I_B + V_{CE} I_C \]

A high value of ODF cannot reduce the CE voltage significantly. However \( V_{BE} \) increases due to increased base current resulting in increased power loss. Once the transistor is saturated, the CE voltage is not reduced in relation to increase in base current. However the power is increased at a high value of ODF, the transistor may be damaged due to thermal runaway. On the other hand if the transistor is under driven \((I_B < I_{BS})\) it may operate in active region, \( V_{CE} \) increases resulting in increased power loss.
PROBLEMS

1. The BJT is specified to have a range of 8 to 40. The load resistance in $R_e = 11\Omega$. The dc supply voltage is $V_{CC} = 200V$ and the input voltage to the base circuit is $V_B = 10V$. If $V_{CE\text{(sat)}} = 1.0V$ and $V_{BE\text{(sat)}} = 1.5V$. Find
   a. The value of $R_B$ that results in saturation with a overdrive factor of 5.
   b. The forced $\beta_f$.
   c. The power loss $P_T$ in the transistor.

Solution

(a) $I_{CS} = \frac{V_{CC} - V_{CE\text{(sat)}}}{R_C} = \frac{200 - 1.0}{11\Omega} = 18.1A$

Therefore $I_{BS} = \frac{I_{CS}}{\beta_{\text{min}}} = \frac{18.1}{8} = 2.2625A$

Therefore $I_B = ODF \times I_{BS} = 11.3125A$

$I_B = \frac{V_B - V_{BE\text{(sat)}}}{R_B}$

Therefore $R_B = \frac{V_B - V_{BE\text{(sat)}}}{I_B} = \frac{10 - 1.5}{11.3125} = 0.715\Omega$

(b) Therefore $\beta_f = \frac{I_{CS}}{I_B} = \frac{18.1}{11.3125} = 1.6$

$c) P_T = V_{BE}I_B + V_{CE}I_C$

$P_T = 1.5 \times 11.3125 + 1.0 \times 18.1$

$P_T = 16.97 + 18.1 = 35.07W$

2. The $\beta$ of a bipolar transistor varies from 12 to 75. The load resistance is $R_e = 1.5\Omega$. The dc supply voltage is $V_{CC} = 40V$ and the input voltage base circuit is $V_B = 6V$. If $V_{CE\text{(sat)}} = 1.2V$, $V_{BE\text{(sat)}} = 1.6V$ and $R_B = 0.7\Omega$ determine
   a. The overdrive factor ODF.
   b. The forced $\beta_f$.
   c. Power loss in transistor $P_T$

Solution

$I_{CS} = \frac{V_{CC} - V_{CE\text{(sat)}}}{R_C} = \frac{40 - 1.2}{1.5} = 25.86A$

$I_{BS} = \frac{I_{CS}}{\beta_{\text{min}}} = \frac{25.86}{12} = 2.15A$

Also $I_B = \frac{V_B - V_{BE\text{(sat)}}}{R_B} = \frac{6 - 1.6}{0.7} = 6.28A$

(a) Therefore $ODF = \frac{I_B}{I_{BS}} = \frac{6.28}{2.15} = 2.92$

Forced $\beta_f = \frac{I_{CS}}{I_B} = \frac{25.86}{6.28} = 4.11$
(c) 
\[ P_T = V_{BE}I_B + V_{CE}I_C \]
\[ P_T = 1.6 \times 6.25 + 1.2 \times 25.86 \]
\[ P_T = 41.032 \text{Watts} \]

(JULY / AUGUST 2004)

3. For the transistor switch as shown in figure
   a. Calculate forced beta, \( \beta_f \) of transistor.
   b. If the manufacturers specified \( \beta \) is in the range of 8 to 40, calculate the minimum overdrive factor (ODF).
   c. Obtain power loss \( P_T \) in the transistor.

![Transistor Switch Diagram](image)

\[ V_B = 10V, \quad R_B = 0.75\Omega, \]
\[ V_{BE(sat)} = 1.5V, \quad R_C = 11\Omega, \]
\[ V_{CE(sat)} = 1V, \quad V_{CC} = 200V \]

Solution

(i) 
\[ I_B = \frac{V_B - V_{BE(sat)}}{R_B} = \frac{10 - 1.5}{0.75} = 11.33A \]
\[ I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{200 - 1.0}{11} = 18.09A \]
Therefore 
\[ I_{BS} = \frac{I_{CS}}{\beta_{min}} = \frac{18.09}{8} = 2.26A \]
\[ \beta_f = \frac{I_{CS}}{I_B} = \frac{18.09}{11.33} = 1.6 \]

(ii) 
\[ ODF = \frac{I_B}{I_{BS}} = \frac{11.33}{2.26} = 5.01 \]

(iii) 
\[ P_T = V_{BE}I_B + V_{CE}I_C = 1.5 \times 11.33 + 1.0 \times 18.09 = 35.085W \]

(JAN / FEB 2005)

4. A simple transistor switch is used to connect a 24V DC supply across a relay coil, which has a DC resistance of 200\( \Omega \). An input pulse of 0 to 5V amplitude is applied through series base resistor \( R_B \) at the base so as to turn on the transistor switch. Sketch the device current waveform with reference to the input pulse.
Calculate
a. $I_{cs}$.

b. Value of resistor $R_b$, required to obtain over drive factor of two.

c. Total power dissipation in the transistor that occurs during the saturation state.

Solution
To sketch the device current waveforms; current through the device cannot rise fast to the saturating level of $I_{cs}$ since the inductive nature of the coil opposes any change in current through it. Rate of rise of collector current can be determined by the time constant $\tau = \frac{L}{R}$. Where L is inductive in Henry of coil and R is resistance of coil. Once steady state value of $I_{cs}$ is reached the coil acts as a short circuit. The collector current stays put at $I_{cs}$ till the base pulse is present.

Similarly once input pulse drops to zero, the current $I_c$ does not fall to zero immediately since inductor will now act as a current source. This current will
now decay at the fall to zero. Also the current has an alternate path and now can flow through the diode.

(i) \[ I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{24 - 0.2}{200} = 0.119A \]

(ii) Value of \( R_B \)

\[ I_{BS} = \frac{I_{CS}}{\beta_{min}} = \frac{0.119}{25} = 4.76mA \]

\[ \therefore I_B = ODF \times I_{BS} = 2 \times 4.76 = 9.52mA \]

\[ \therefore R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{5 - 0.7}{9.52} = 450\Omega \]

(iii) \[ P_I = V_{BE(sat)} \times I_B + V_{CE(sat)} \times I_{CS} = 0.7 \times 9.52 + 0.2 \times 0.119 = 6.68W \]

**SWITCHING CHARACTERISTICS**

A forward biased p-n junction exhibits two parallel capacitances; a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased p-n junction has only depletion capacitance. Under steady state the capacitances do not play any role. However under transient conditions, they influence turn-on and turn-off behavior of the transistor.

**TRANSIENT MODEL OF BJT**

![Transistor Models](image)

(a) Model with current gain  
(b) Model with transconductance

**Fig. 7: Transient Model of BJT**
Due to internal capacitances, the transistor does not turn on instantly. As the voltage $V_B$ rises from zero to $V_1$ and the base current rises to $I_{B1}$, the collector current does not respond immediately. There is a delay known as delay time $t_d$, before any collector current flows. The delay is due to the time required to charge up the BEJ to the forward bias voltage $V_{BE}(0.7V)$. The collector current rises to the steady value of $I_{CS}$ and this time is called rise time $t_r$.

The base current is normally more than that required to saturate the transistor. As a result excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge which is called the saturating charge is proportional to the excess base drive.

This extra charge which is called the saturating charge, is proportional to the excess base drive and the corresponding current $I_c$.

$$I_c = I_B - I_{CS} = ODF \cdot I_{BS} - I_{BS} = I_{BS} (ODF - 1)$$

Saturating charge $Q_s = \tau_s I_c = \tau_s I_{BS} (ODF - 1)$ where $\tau_s$ is known as the storage time constant.

When the input voltage is reversed from $V_1$ to $-V_2$, the reverse current $-I_{B2}$ helps to discharge the base. Without $-I_{B2}$ the saturating charge has to be removed entirely due to recombination and the storage time $t_s$ would be longer. Once the extra charge is removed, BEJ charges to the input voltage $-V_2$ and the base current falls to zero. $t_f$ depends on the time constant which is determined by the reverse biased BEJ capacitance.

**Fig. 8: Switching Times of BJT**
\[ \therefore \quad t_{\text{on}} = t_d + t_r \\
\quad t_{\text{off}} = t_s + t_f \]

**PROBLEMS**

1. For a power transistor, typical switching waveforms are shown. The various parameters of the transistor circuit are as under \( V_c = 220\, V \), \( V_{CE(sat)} = 2\, V \), \( I_{CS} = 80\, A \), \( t_d = 0.4\, \mu s \), \( t_r = 1\, \mu s \), \( t_s = 0.5 \, \mu s \), \( t_f = 2\, \mu s \), \( t_0 = 40\, \mu s \), \( f = 5\, \text{KHz} \), \( I_{CEO} = 2\, \text{mA} \). Determine average power loss due to collector current during \( t_{\text{on}} \) and \( t_{\text{off}} \). Find also the peak instantaneous power loss, due to collector current during turn-on time.

**Solution**

During delay time, the time limits are \( 0 \leq t \leq t_d \). Figure shows that in this time \( i_c(t) = I_{CEO} \) and \( V_{CE}(t) = V_{CC} \). Therefore instantaneous power loss during delay time is
\[
P_{\text{d}}(t) = i_c V_{CE} = I_{CEO} V_{CC} = 2 \times 10^{-3} \times 220 = 0.44\, \text{W} \]

Average power loss during delay time \( 0 \leq t \leq t_d \) is given by
\[
P_{\text{d}} = \frac{1}{T_d} \int_0^{t_d} i_c(t) v_{CE}(t) \, dt
\]
\[
P_{\text{d}} = \frac{1}{T} \int_0^{t_d} I_{CEO} V_{CC} \, dt
\]
\[
P_{\text{d}} = f I_{CEO} V_{CC} t_d
\]
\[
P_{\text{d}} = 5 \times 10^3 \times 2 \times 10^{-3} \times 220 \times 0.4 \times 10^{-6} = 0.88\, \text{mW} \]

During rise time \( 0 \leq t \leq t_r \)
\[
i_c(t) = \frac{I_{CS}}{t_r} t
\]
\[
v_{CE}(t) = \left[ V_{CC} - \left( \frac{V_{CC} - V_{CE(sat)}}{t_r} \right) t \right]
\]
\[
v_{CE}(t) = V_{CC} + \left( V_{CE(sat)} - V_{CC} \right) \frac{t}{t_r}
\]

Therefore average power loss during rise time is
\[
P_{r} = \frac{1}{T_r} \int_0^{t_r} \left[ V_{CC} + \left( V_{CE(sat)} - V_{CC} \right) \frac{t}{t_r} \right] \, dt
\]
\[
P_{r} = f I_{CS} t_r \left[ \frac{V_{CC}}{2} - \frac{V_{CC} - V_{CES}}{3} \right]
\]
\[
P_{r} = 5 \times 10^3 \times 80 \times 1 \times 10^{-6} \left[ \frac{220}{2} - \frac{220 - 2}{3} \right] = 14.933\, \text{W}
\]

Instantaneous power loss during rise time is
\[
P_{r}(t) = \frac{I_{CS}}{t_r} t \left[ V_{CC} - \frac{V_{CC} - V_{CE(sat)}}{t_r} t \right]
\]
\[ P_r(t) = \frac{I_{CS}}{t_r} t V_{CC} - \frac{I_{CS}^2}{t_r^2} \left[ V_{CC} - V_{CE(sat)} \right] \]

Differentiating the above equation and equating it to zero will give the time \( t_m \) at which instantaneous power loss during \( t_r \) would be maximum.

Therefore
\[ \frac{dP_r(t)}{dt} = \frac{I_{CS} V_{CC}}{t_r} - \frac{I_{CS}^2 2t}{t_r^2} \left[ V_{CC} - V_{CE(sat)} \right] \]

At \( t = t_m \),
\[ \frac{dP_r(t)}{dt} = 0 \]

Therefore
\[ 0 = \frac{I_{CS} V_{CC}}{t_r} - \frac{2I_{CS} t_m}{t_r^2} \left[ V_{CC} - V_{CE(sat)} \right] \]

\[ \frac{I_{CS} V_{CC}}{t_r} = \frac{2I_{CS} t_m}{t_r^2} \left[ V_{CC} - V_{CE(sat)} \right] \]

\[ \frac{t_r V_{CC}}{2} = t_m \left[ V_{CC} - V_{CE(sat)} \right] \]

Therefore
\[ t_m = \frac{t_r V_{CC}}{2 \left[ V_{CC} - V_{CE(sat)} \right]} \]

Therefore
\[ t_m = \frac{V_{CC} t_r}{2 \left[ V_{CC} - V_{CE(sat)} \right]} = \frac{220 \times 1 \times 10^{-6}}{2 \left[ 200 - 2 \right]} = 0.5046 \mu s \]

Peak instantaneous power loss \( P_{im} \) during rise time is obtained by substituting the value of \( t = t_m \) in equation (1) we get

\[ P_{im} = \frac{I_{CS}}{t_r} \frac{V_{CC}^2}{2} t_r - \frac{I_{CS}^2 \left( V_{CC} t_r \right)^2}{t_r^2} \left[ V_{CC} - V_{CE(sat)} \right] \]

\[ P_{im} = \frac{80 \times 220^2}{4 \left[ 220 - 2 \right]} = 4440.4W \]

Total average power loss during turn-on
\[ P_{on} = Pd + P_r = 0.00088 + 14.933 = 14.9339W \]

During conduction time \( 0 \leq t \leq t_n \)
\[ i_c(t) = I_{CS} \quad \text{&} \quad v_{CE}(t) = V_{CE(sat)} \]

Instantaneous power loss during \( t_n \) is
\[ P_n(t) = i_c v_{CE} = I_{CS} V_{CE(sat)} = 80 \times 2 = 160W \]

Average power loss during conduction period is
\[ P_n = \frac{1}{T} \int_0^T i_c v_{CE} dt = f I_{CS} V_{CES} t_n = 5 \times 10^3 \times 80 \times 2 \times 50 \times 10^{-6} = 40W \]
PERFORMANCE PARAMETERS

DC gain \( h_{FE} \ \beta = \frac{I_C}{I_B}[V_{CE}] \): Gain is dependent on temperature. A high gain would reduce the values of forced \( \beta \) & \( V_{CE(sat)} \).

\( V_{CE(sat)} \): A low value of \( V_{CE(sat)} \) will reduce the on-state losses. \( V_{CE(sat)} \) is a function of the collector circuit, base current, current gain and junction temperature. A small value of forced \( \beta \) decreases the value of \( V_{CE(sat)} \).

\( V_{BE(sat)} \): A low value of \( V_{BE(sat)} \) will decrease the power loss in the base emitter junction. \( V_{BE(sat)} \) increases with collector current and forced \( \beta \).

Turn-on time \( t_{on} \): The turn-on time can be decreased by increasing the base drive for a fixed value of collector current. \( t_d \) is dependent on input capacitance does not change significantly with \( I_c \). However \( t_c \) increases with increase in \( I_c \).

Turn off time \( t_{off} \): The storage time \( t_s \) is dependent on over drive factor and does not change significantly with \( I_c \). \( t_s \) is a function of capacitance and increases with \( I_c \). \( t_s \) & \( t_f \) can be reduced by providing negative base drive during turn-off. \( t_f \) is less sensitive to negative base drive.

Cross-over \( t_c \): The crossover time \( t_c \) is defined as the interval during which the collector voltage \( V_{CE} \) rises from 10% of its peak off state value and collector current. \( I_c \) falls to 10% of its on-state value. \( t_c \) is a function of collector current negative base drive.

Switching Limits

SECOND BREAKDOWN

It is a destructive phenomenon that results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient the excessive localized heating may damage the transistor. Thus secondary breakdown is caused by a localized thermal runaway. The SB occurs at certain combinations of voltage, current and time. Since time is involved, the secondary breakdown is basically an energy dependent phenomenon.

FORWARD BIASED SAFE OPERATING AREA FBSOA

During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power handling capability of a transistor. The manufacturer usually provide the FBSOA curves under specified test conditions. FBSOA indicates the \( I_c - V_{ce} \) limits of the transistor and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.
Fig. 9: FBSOA of Power BJT

The dc FBSOA is shown as shaded area and the expansion of the area for pulsed operation of the BJT with shorter switching times which leads to larger FBSOA. The second break down boundary represents the maximum permissible combinations of voltage and current without getting into the region of $i_c - v_{ce}$ plane where second breakdown may occur. The final portion of the boundary of the FBSOA is breakdown voltage limit $BV_{CEO}$.

REVERSE BIASED SAFE OPERATING AREA RBSoA

During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-emitter junction reverse biased. The collector emitter voltage must be held to a safe level at or below a specified value of collector current. The manufacturer provide $I_c - V_{ce}$ limits during reverse-biased turn off as reverse biased safe area (RBSOA).

Fig. 10: RBSOA of a Power BJT
The area encompassed by the RBSOA is some what larger than FBSOA because of the extension of the area of higher voltages than $BV_{CEO}$ upto $BV_{CBO}$ at low collector currents. This operation of the transistor upto higher voltage is possible because the combination of low collector current and reverse base current has made the beta so small that break down voltage rises towards $BV_{CBO}$.

**POWER DERATING**

The thermal equivalent is shown. If the total average power loss is $P_T$,

The case temperature is \[ T_c = T_j - P_T T_{jc}. \]

The sink temperature is \[ T_s = T_c - P_T T_{CS}. \]

The ambient temperature is \[ T_A = T_S - P_T R_{SA} \text{ and } T_j - T_A = P_T \left( R_{jc} + R_{cs} + R_{SA} \right) \]

$R_{jc}$ : Thermal resistance from junction to case $^\circ\Omega$.

$R_{cs}$ : Thermal resistance from case to sink $^\circ\Omega$.

$R_{SA}$ : Thermal resistance from sink to ambient $^\circ\Omega$.

The maximum power dissipation in $P_T$ is specified at $T_c = 25^\circ C$.

![Fig. 11: Thermal Equivalent Circuit of Transistor](image)

**BREAK DOWN VOLTAGES**

A break down voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted or biased in either forward or reverse direction.

$BV_{SUS}$ : The maximum voltage between the collector and emitter that can be sustained across the transistor when it is carrying substantial collector current.

$BV_{CEO}$ : The maximum voltage between the collector and emitter terminal with base open circuited.

$BV_{CBO}$ : This is the collector to base break down voltage when emitter is open circuited.
BASE DRIVE CONTROL

This is required to optimize the base drive of transistor. Optimization is required to increase switching speeds. \( t_{on} \) can be reduced by allowing base current peaking during turn-on, \( \beta_f = \frac{I_{CS}}{I_B} \left[ \text{forced} \beta \right] \) resulting in low forces \( \beta \) at the beginning. After turn on, \( \beta_f \) can be increased to a sufficiently high value to maintain the transistor in quasi-saturation region. \( t_{off} \) can be reduced by reversing base current and allowing base current peaking during turn off since increasing \( I_{B2} \) decreases storage time.

A typical waveform for base current is shown.

Fig. 12: Base Drive Current Waveform

Some common types of optimizing base drive of transistor are

- Turn-on Control.
- Turn-off Control.
- Proportional Base Control.
- Antisaturation Control

TURN-ON CONTROL

When input voltage is turned on, the base current is limited by resistor \( R_1 \) and therefore initial value of base current is \( I_{BO} = \frac{V_1 - V_{BE}}{R_1} \), \( I_{BF} = \frac{V_1 - V_{BE}}{R_1 + R_2} \).

Capacitor voltage \( V_C = V_1 \frac{R_2}{R_1 + R_2} \).
Therefore \[ \tau_1 = \left( \frac{R_1 R_2}{R_1 + R_2} \right) C_1 \]

Once input voltage \( v_b \) becomes zero, the base-emitter junction is reverse biased and \( C_1 \) discharges through \( R_2 \). The discharging time constant is \( \tau_2 = R_2 C_1 \). To allow sufficient charging and discharging time, the width of base pulse must be \( t_1 \geq 5 \tau_1 \) and off period of the pulse must be \( t_2 \geq 5 \tau_2 \). The maximum switching frequency is \( f_s = \frac{1}{T} = \frac{1}{t_1 + t_2} = \frac{0.2}{\tau_1 + \tau_2} \).

**TURN-OFF CONTROL**

If the input voltage is changed to during turn-off the capacitor voltage \( V_C \) is added to \( V_2 \) as reverse voltage across the transistor. There will be base current peaking during turn-off. As the capacitor \( C_1 \) discharges, the reverse voltage will be reduced to a steady state value, \( V_2 \). If different turn-on and turn-off characteristics are required, a turn-off circuit using \( (C_2, R_3, R_4) \) may be added. The diode \( D_1 \) isolates the forward base drive circuit from the reverse base drive circuit during turn off.

![Figure 8-16](image)

**Fig: 14. Base current peaking during turn-on and turn-off**

**PROPORTIONAL BASE CONTROL**

This type of control has advantages over the constant drive circuit. If the collector current changes due to change in load demand, the base drive current is changed in proportion to collector current.

When switch \( S_1 \) is turned on a pulse current of short duration would flow through the base of transistor \( Q_1 \) and \( Q_1 \) is turned on into saturation. Once the collector current starts to flow, a corresponding base current is induced due to transformer action. The transistor would latch on itself and \( S_1 \) can be turned off. The turns ratio is \( \frac{N_2}{N_1} = \frac{I_C}{I_B} = \beta \). For proper operation of the circuit, the magnetizing current which must be much smaller than the collector current should be as small as possible. The switch \( S_1 \) can be implemented by a small signal transistor and additional arrangement is necessary to discharge capacitor \( C_1 \) and reset the transformer core during turn-off of the power transistor.
If a transistor is driven hard, the storage time which is proportional to the base current increases and the switching speed is reduced. The storage time can be reduced by operating the transistor in soft saturation rather than hard saturation. This can be accomplished by clamping CE voltage to a pre-determined level and the collector current is given by 
\[ I_C = \frac{V_{CC} - V_{CM}}{R_C} \]
Where \( V_{CM} \) is the clamping voltage and \( V_{CM} > V_{CE(sat)} \).

The base current which is adequate to drive the transistor hard, can be found from 
\[ I_B = I_1 = \frac{V_B - V(D) - V_{BE}}{R_B} \]
and the corresponding collector current is 
\[ I_C = I_L = \beta I_B \]

Writing the loop equation for the input base circuit,
\[ V_{ab} = V_{D_1} + V_{BE} \]
Similarly 
\[ V_{ab} = V_{D_2} + V_{CE} \]
Therefore 
\[ V_{CE} = V_{BE} + V_{D_1} - V_{D_2} \]
For clamping 
\[ V_{D_1} > V_{D_2} \]
Therefore 
\[ V_{CE} = 0.7 + \ldots \]

This means that the CE voltage is raised above saturation level and there are no excess carriers in the base and storage time is reduced.
The load current is \( I_L = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE} - V_{D_1} + V_{D_2}}{R_C} \) and the collector current with clamping is \( I_C = \beta I_B = \beta \left( I_t - I_c + I_L \right) = \frac{\beta}{1 + \beta} (I_t + I_L) \).

For clamping, \( V_{D_1} > V_{D_2} \) and this can be accomplished by connecting two or more diodes in place of \( D_1 \). The load resistance \( R_C \) should satisfy the condition \( \beta I_B > I_L \), \( \beta I_B R_C > \left( V_{CC} - V_{BE} - V_{D_1} + V_{D_2} \right) \).

The clamping action thus results a reduced collector current and almost elimination of the storage time. At the same time, a fast turn-on is accomplished. However, due to increased \( V_{CE} \), the on-state power dissipation in the transistor is increased, whereas the switching power loss is decreased.

**ADVANTAGES OF BJT’S**

- BJT’s have high switching frequencies since their turn-on and turn-off time are low.
- The turn-on losses of a BJT are small.
- BJT has controlled turn-on and turn-off characteristics since base drive control is possible.
- BJT does not require commutation circuits.

**DEMERITS OF BJT**

- Drive circuit of BJT is complex.
- It has the problem of charge storage which sets a limit on switching frequencies. It cannot be used in parallel operation due to problems of negative temperature coefficient.
POWER MOSFETS

INTRODUCTION TO FET'S

FET's use field effect for their operation. FET is manufactured by diffusing two areas of p-type into the n-type semiconductor as shown. Each p-region is connected to a gate terminal; the gate is a p-region while source and drain are n-region. Since it is similar to two diodes one is a gate source diode and the other is a gate drain diode.

![Fig:1: Schematic symbol of JFET](image)

In BJT’s we forward bias the B-E diode but in a JFET, we always reverse bias the gate-source diode. Since only a small reverse current can exist in the gate lead. Therefore $I_G = 0$, therefore $R_{in} = \infty$ (ideal).

The term field effect is related to the depletion layers around each p-region as shown. When the supply voltage $V_{DD}$ is applied as shown it forces free electrons to flow
from source to drain. With gate reverse biased, the electrons need to flow from source to drain, they must pass through the narrow channel between the two depletion layers. The more the negative gate voltage is the tighter the channel becomes.

Therefore JFET acts as a voltage controlled device rather than a current controlled device.

JFET has almost infinite input impedance but the price paid for this is loss of control over the output current, since JFET is less sensitive to changes in the output voltage than a BJT.

**JFET CHARACTERISTICS**

\[ I_{ds} = \text{drain-source current} \quad V_{ds} = \text{drain-source voltage} \quad V_{gs} = \text{gate-source voltage} \]

*Characteristic curves for a typical N-channel JFET.*
The maximum drain current out of a JFET occurs when $V_{GS} = 0$. As $V_{DS}$ is increased for 0 to a few volts, the current will increase as determined by ohms law. As $V_{DS}$ approaches $V_p$ the depletion region will widen, carrying a noticeable reduction in channel width. If $V_{DS}$ is increased to a level where the two depletion region would touch a pinch-off will result. $I_D$ now maintains a saturation level $I_{DSS}$. Between 0 volts and pinch off voltage $V_p$ is the ohmic region. After $V_p$, the regions constant current or active region.

If negative voltage is applied between gate and source the depletion region similar to those obtained with $V_{GS} = 0$ are formed but at lower values of $V_{DS}$. Therefore saturation level is reached earlier.

We can find two important parameters from the above characteristics

- $r_{ds} = \text{drain to source resistance} = \frac{\Delta V_{DS}}{\Delta I_D}$
- $g_m = \text{transconductance of the device} = \frac{\Delta I_D}{\Delta V_{GS}}$
- The gain of the device, amplification factor $\mu = r_{ds} g_m$. 

SHOCKLEY EQUATION

The FET is a square law device and the drain current $I_D$ is given by the Shockley equation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

and

$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

MOSFET

MOSFET stands for metal oxide semiconductor field effect transistor. There are two types of MOSFET

- Depletion type MOSFET
- Enhancement type MOSFET

DEPLETION TYPE MOSFET

CONSTRUCTION

Symbol of n-channel depletion type MOSFET

It consists of a highly doped p-type substrate into which two blocks of heavily doped n-type material are diffused to form a source and drain. A n-channel is formed by diffusing between source and drain. A thin layer of $SiO_2$ is grown over the entire surface and holes are cut in $SiO_2$ to make contact with n-type blocks. The gate is also connected to a metal contact surface but remains insulated from the n-channel by the $SiO_2$ layer. $SiO_2$ layer results in an extremely high input impedance of the order of $10^{10}$ to $10^{15}$Ω for this area.
Fig. 4: Structure of n-channel depletion type MOSFET

OPERATION

When $V_{GS} = 0\,V$ and $V_{DS}$ is applied and current flows from drain to source similar to JFET. When $V_{GS} = -1\,V$, the negative potential will tend to pressure electrons towards the p-type substrate and attracts hole from p-type substrate. Therefore recombination occurs and will reduce the number of free electrons in the n-channel for conduction. Therefore with increased negative gate voltage $I_D$ reduces.

For positive values, $V_{gs}$, additional electrons from p-substrate will flow into the channel and establish new carriers which will result in an increase in drain current with positive gate voltage.

DRAIN CHARACTERISTICS
TRANSFER CHARACTERISTICS

![Transfer Characteristic Graph]

**ENHANCEMENT TYPE MOSFET**

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET’s and depletion type MOSFET.

**BASIC CONSTRUCTION**

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO₂ layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.

---

**Fig. 5: Structure of n-channel enhancement type MOSFET**
OPERATION

If $V_{gs} = 0V$ and a voltage is applied between the drain and source, the absence of an n-channel will result in a current of effectively zero amperes. With $V_{ds}$ set at some positive voltage and $V_{gs}$ set at 0V, there are two reverse biased p-n junction between the n-doped regions and p substrate to oppose any significant flow between drain and source.

If both $V_{ds}$ and $V_{gs}$ have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of $SiO_2$ layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the $SiO_2$ layer. The negative carriers will not be absorbed due to insulating $SiO_2$ layer, forming an inversion layer which results in current flow from drain to source.

The level of $V_{gs}$ that results in significant increase in drain current is called threshold voltage $V_T$. As $V_{gs}$ increases the density of free carriers will increase resulting in increased level of drain current. If $V_{gs}$ is constant $V_{ds}$ is increased; the drain current will eventually reach a saturation level as occurred in JFET.

DRAIN CHARACTERISTICS
POWER MOSFET’S

Power MOSFET’s are generally of enhancement type only. This MOSFET is turned ‘ON’ when a voltage is applied between gate and source. The MOSFET can be turned ‘OFF’ by removing the gate to source voltage. Thus gate has control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFET’s are very small. Hence they operate at very high frequencies; hence MOSFET’s are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFET are very simple. The paralleling of MOSFET’s is easier due to their positive temperature coefficient. But MOSFTS’s have high on-state resistance hence for higher currents; losses in the MOSFET’s are substantially increased. Hence MOSFET’s are used for low power applications.

CONSTRUCTION
Power MOSFET’s have additional features to handle larger powers. On the $n^+$ substrate high resistivity $n^-$ layer is epitaxially grown. The thickness of $n^-$ layer determines the voltage blocking capability of the device. On the other side of $n^+$ substrate, a metal layer is deposited to form the drain terminal. Now $p^-$ regions are diffused in the epitaxially grown $n^-$ layer. Further $n^+$ regions are diffused in the $p^-$ regions as shown. $SiO_2$ layer is added, which is then etched so as to fit metallic source and gate terminals.

A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

When gate circuit voltage is zero and $V_{DD}$ is present, $n^+ - p^-$ junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons from $n^-$ channel in the $p^-$ regions. Therefore a current from drain to source is established.

Power MOSFET conduction is due to majority carriers therefore time delays caused by removal of recombination of minority carriers is removed.

Because of the drift region the ON state drop of MOSFET increases. The thickness of the drift region determines the breakdown voltage of MOSFET. As seen a parasitic BJT is formed, since emitter base is shorted to source it does not conduct.

**SWITCHING CHARACTERISTICS**

The switching model of MOSFET’s is as shown in the figure 6(a). The various inter electrode capacitance of the MOSFET which cannot be ignored during high frequency switching are represented by $C_{gs}, C_{gd} & C_{ds}$. The switching waveforms are as shown in figure 7. The turn on time $t_o$ is the time that is required to charge the input capacitance to the threshold voltage level. The rise time $t_r$ is the gate charging time from this threshold level to the full gate voltage $V_{gsp}$. The turn off delay time $t_{off}$ is the time required for the input capacitance to discharge from overdriving the voltage $V_1$ to the pinch off region. The fall time is the time required for the input capacitance to discharge from pinch off region to the threshold voltage. Thus basically switching ON and OFF depend on the charging time of the input gate capacitance.
The turn-on time can be reduced by connecting a RC circuit as shown to charge the capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is

\[ I_G = \frac{V_G}{R_s} \]

The steady state value of gate voltage is

\[ V_{gs} = \frac{R_G V_G}{R_s + R_t + R_G} \]

Where \( R_s \) is the internal resistance of gate drive force.
COMPARISON OF MOSFET WITH BJT

- Power MOSFETs have lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching loss but lower conduction loss. So at high frequency applications power MOSFET is the obvious choice. But at lower operating frequencies BJT is superior.
- MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFET’s easy. If a MOSFET shares increased current initially, it heats up faster, its resistance increases and this increased resistance causes the current to shift to other devices in parallel. A BJT is a negative temperature coefficient, so current shaving resistors are necessary during parallel operation of BJT’s.
- In MOSFET secondary breakdown does not occur because it have positive temperature coefficient. But BJT exhibits negative temperature coefficient which results in secondary breakdown.
- Power MOSFET’s in higher voltage ratings have more conduction losses.
- Power MOSFET’s have lower ratings compared to BJT’s. Power MOSFET’s → 500V to 140A, BJT → 1200V, 800A.
MOSIGT OR IGBT

The metal oxide semiconductor insulated gate transistor or IGBT combines the advantages of BJT's and MOSFET's. Therefore an IGBT has high input impedance like a MOSFET and low-on state power loss as in a BJT. Further IGBT is free from second breakdown problem present in BJT.

IGBT BASIC STRUCTURE AND WORKING

It is constructed virtually in the same manner as a power MOSFET. However, the substrate is now a $p^+$ layer called the collector.

When gate is positive with respect to positive with respect to emitter and with gate emitter voltage greater than $V_{GSTH}$, an n channel is formed as in case of power MOSFET. This $n^-$ channel short circuits the $n^-$ region with $n^+$ emitter regions.

An electron movement in the $n^-$ channel in turn causes substantial hole injection from $p^+$ substrate layer into the epitaxially $n^-$ layer. Eventually a forward current is established.
The three layers $p^+$, $n^-$ and $p$ constitute a pnp transistor with $p^+$ as emitter, $n^-$ as base and $p$ as collector. Also $n^-$, $p$ and $n^+$ layers constitute a npn transistor. The MOSFET is formed with input gate, emitter as source and $n^-$ region as drain. Equivalent circuit is as shown below.

(b) Equivalent circuit

(c) Simplified circuit
Also $p$ serves as collector for pnp device and also as base for npn transistor. The two pnp and npn is formed as shown.

When gate is applied ($V_{GS} > V_{GSth}$) MOSFET turns on. This gives the base drive to $T_1$. Therefore $T_1$ starts conducting. The collector of $T_1$ is base of $T_2$. Therefore regenerative action takes place and large number of carriers are injected into the $n^-$ drift region. This reduces the ON-state loss of IGBT just like BJT.

When gate drive is removed IGBT is turn-off. When gate is removed the induced channel will vanish and internal MOSFET will turn-off. Therefore $T_1$ will turn-off it $T_2$ turns off.

Structure of IGBT is such that $R_i$ is very small. If $R_i$ small $T_i$ will not conduct therefore IGBT’s are different from MOSFET’s since resistance of drift region reduces when gate drive is applied due to $p^+$ injecting region. Therefore ON state IGBT is very small.

**IGBT CHARACTERISTICS**

**STATIC CHARACTERISTICS**

![IGBT bias circuit](image)

**Fig. 9: IGBT bias circuit**

**Static V-I characteristics ($I_C$ versus $V_{CE}$)**

Same as in BJT except control is by $V_{GE}$. Therefore IGBT is a voltage controlled device.

**Transfer Characteristics ($I_C$ versus $V_{GE}$)**

Identical to that of MOSFET. When $V_{GE} < V_{GET}$, IGBT is in off-state.
APPLICATIONS

Widely used in medium power applications such as DC and AC motor drives, UPS systems, Power supplies for solenoids, relays and contractors.

Though IGBT’s are more expensive than BJT’s, they have lower gate drive requirements, lower switching losses. The ratings up to 1200V, 500A.

SERIES AND PARALLEL OPERATION

Transistors may be operated in series to increase their voltage handling capability. It is very important that the series-connected transistors are turned on and off simultaneously. Otherwise, the slowest device at turn-on and the fastest devices at turn-off will be subjected to the full voltage of the collector-emitter circuit and the particular device may be destroyed due to high voltage. The devices should be matched for gain, transconductance, threshold voltage, on state voltage, turn-on time, and turn-off time. Even the gate or base drive characteristics should be identical.

Transistors are connected in parallel if one device cannot handle the load current demand. For equal current sharings, the transistors should be matched for gain, transconductance, saturation voltage, and turn-on time and turn-off time. But in practice, it is not always possible to meet these requirements. A reasonable amount of current sharing (45 to 55% with two transistors) can be obtained by connecting resistors in series with the emitter terminals as shown in the figure 10.

![Diagram of Parallel Connection of Transistors](image)

**Fig. 10: Parallel connection of Transistors**
The resistor will help current sharing under steady state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors. If the current through $Q_1$ rises, the $I(dI/dt)$ across $L_4$ increases, and a corresponding voltage of opposite polarity is induced across inductor $L_2$. The result is low impedance path, and the current is shifted to $Q_2$. The inductors would generate voltage spikes and they may be expensive and bulky, especially at high currents.

![Fig. 11: Dynamic current sharing](image)

BJTs have a negative temperature coefficient. During current sharing, if one BJT carries more current, its on-state resistance decreases and its current increases further, whereas MOSFETS have positive temperature coefficient and parallel operation is relatively easy. The MOSFET that initially draws higher current heats up faster and its on-state resistance increases, resulting in current shifting to the other devices. IGBTs require special care to match the characteristics due to the variations of the temperature coefficients with the collector current.

PROBLEM
1. Two MOSFETS which are connected in parallel carry a total current of $I_T = 20\,\text{A}$. The drain to source voltage of MOSFET $M_1$ is $V_{DS1} = 2.5\,\text{V}$ and that of MOSFET $M_2$ is $V_{DS2} = 3\,\text{V}$. Determine the drain current of each transistor and difference in current sharing if the current sharing series resistances are (a) $R_{s1} = 0.3\,\Omega$ and $R_{s2} = 0.2\,\Omega$, and (b) $R_{s1} = R_{s2} = 0.5\,\Omega$.

Solution
(a) $I_{D1} + I_{D2} = I_T \,\text{and} \, V_{DS1} + I_{D1}R_{s1} = V_{DS2} + I_{D2}R_{s2} = R_{s2}(I_T - I_D)$

\[
I_{D1} = \frac{V_{DS2} - V_{DS1} + I_T R_{s2}}{R_{s1} + R_{s2}}
\]

\[
I_{D1} = \frac{3 - 2.5 + 20 \times 0.2}{0.3 + 0.2} = 9\,\text{A} \quad \text{or} \quad 45%
\]

\[
I_{D2} = 20 - 9 = 11\,\text{A} \quad \text{or} \quad 55%
\]

$\Delta I = 55 - 45 = 10\%$
(b) \[ I_{D1} = \frac{3 - 2.5 + 20 \times 0.5}{0.5 + 0.5} = 10.5A \quad \text{or} \quad 52.5\% \]
\[ I_{D2} = 20 - 10.5 = 9.5A \quad \text{or} \quad 47.5\% \]
\[ \Delta I = 52.5 - 47.5 = 5\% \]

\[ \frac{di}{dt} \text{ AND } \frac{dv}{dt} \text{ LIMITATIONS} \]

Transistors require certain turn-on and turn-off times. Neglecting the delay time \( t_d \) and the storage time \( t_s \), the typical voltage and current waveforms of a BJT switch is shown below.

During turn-on, the collector rise and the \( \frac{di}{dt} \) is

\[ \frac{di}{dt} = \frac{I_L}{t_r} = \frac{I_{CS}}{t_r} \quad \ldots (1) \]

During turn off, the collector emitter voltage must rise in relation to the fall of the collector current, and is

\[ \frac{dv}{dt} = \frac{V_s}{t_f} = \frac{V_{CC}}{t_f} \quad \ldots (2) \]

The conditions \( \frac{di}{dt} \) and \( \frac{dv}{dt} \) in equation (1) and (2) are set by the transistor switching characteristics and must be satisfied during turn on and turn off. Protection circuits are normally required to keep the operating \( \frac{di}{dt} \) and \( \frac{dv}{dt} \) within the allowable limits of transistor. A typical switch with \( \frac{di}{dt} \) and \( \frac{dv}{dt} \) protection is shown in figure (a), with operating wave forms in figure (b). The RC network across the transistor is known as the snubber circuit or snubber and limits the \( \frac{dv}{dt} \). The inductor \( L_s \), which limits the \( \frac{di}{dt} \), is sometimes called series snubber.
Let us assume that under steady state conditions the load current $I_L$ is free wheeling through diode $D_m$, which has negligible reverse recovery time. When transistor $Q_1$ is turned on, the collector current rises and current of diode $D_m$ falls, because $D_m$ will behave as short circuited. The equivalent circuit during turn on is shown in figure below.

The turn on $\frac{di}{dt}$ is

$$\frac{di}{dt} = \frac{V_s}{L_s} \quad \text{(3)}$$

Equating equations (1) and (3) gives the value of $L_s$

$$L_s = \frac{V t_f}{I_L} \quad \text{(4)}$$

During turn off, the capacitor $C_s$ will charge by the load current and the equivalent circuit is shown in figure (4). The capacitor voltage will appear across the transistor and the $dv/dt$ is

$$\frac{dv}{dt} = \frac{I_L}{C_s} \quad \text{(5)}$$

Equating equation (2) to equation (5) gives the required value of capacitance,

$$C_s = \frac{I_L t_f}{V_s} \quad \text{(6)}$$
Once the capacitor is charged to $V_i$, the freewheeling diode will turn on. Due to the energy stored in $L_i$, there will be damped resonant circuit as shown in figure (5). The RLC circuit is normally made critically damped to avoid oscillations. For unity critical damping, $\delta = 1$, and equation $\delta = \frac{\alpha}{\omega_0} = \frac{R}{2\sqrt{L/C}}$ yields

$$R_s = 2\sqrt{\frac{L_i}{C_i}}$$

The capacitor $C_i$ has to discharge through the transistor and the increase the peak current rating of the transistor. The discharge through the transistor can be avoided by placing resistor $R_s$ across $C_i$ instead of placing $R_s$ across $D_i$.

The discharge current is shown in figure below. When choosing the value of $R_s$, the discharge time, $R_sC_i = \tau$, should also be considered. A discharge time of one third the switching period, $T_s$ is usually adequate.

$$3R_sC_i = T_s = \frac{1}{f_s}$$

$$R_s = \frac{1}{3f_sC_s}$$

**ISOLATION OF GATE AND BASE DRIVES**

**Necessity**

Driver circuits are operated at very low power levels. Normally the gating circuit are digital in nature which means the signal levels are 3 to 12 volts. The gate and base drives are connected to power devices which operate at high power levels.

**Illustration**

The logic circuit generates four pulses; these pulses have common terminals. The terminal $g_1$, which has a voltage of $V_{g_1}$, with respect to terminal $C$, cannot be connected directly to gate terminal $G$, therefore $V_{g_1}$ should be applied between $G_1$ & $S_1$ of transistor $Q_1$. Therefore there is need for isolation between logic circuit and power transistor.
There are two ways of floating or isolating control or gate signal with respect to ground.

- Pulse transformers
- Optocouplers

**PULSE TRANSFORMERS**

Pulse transformers have one primary winding and can have one or more secondary windings.

Multiple secondary windings allow simultaneous gating signals to series and parallel connected transistors. The transformer should have a very small leakage inductance and the rise time of output should be very small.

The transformer would saturate at low switching frequency and output would be distorted.
OPTOCOUPLERS

Optocouplers combine infrared LED and a silicon photo transistor. The input signal is applied to ILED and the output is taken from the photo transistor. The rise and fall times of photo transistor are very small with typical values of turn on time = 2.5µs and turn off of 300ns. This limits the high frequency applications. The photo transistor could be a darlington pair. The phototransistor require separate power supply and add to complexity and cost and weight of driver circuits.