GCEM

Gopalan College of Engineering and Management

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NOTES

SUBJECT: DIGITAL SIGNAL PROCESSING

SUBJECT CODE: 21EC42

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Module-5

Digital signal processor

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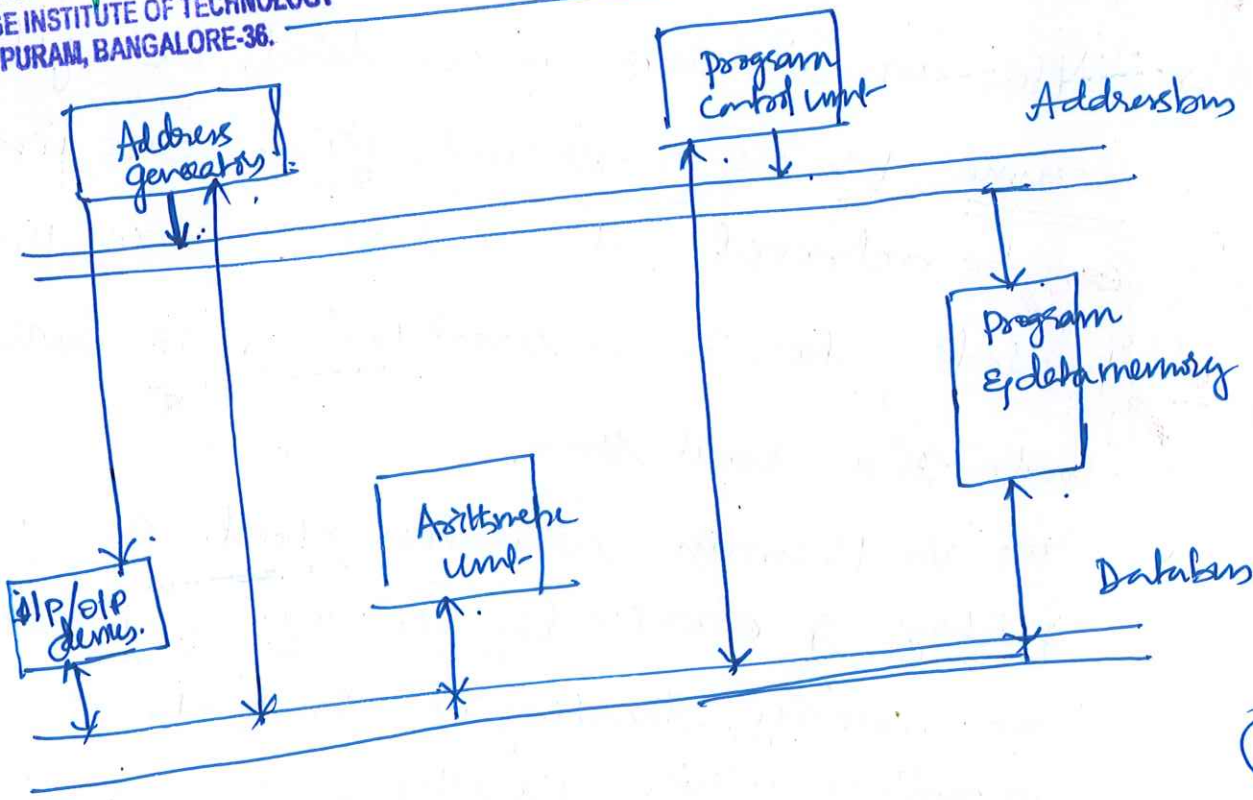
* Unlike µprocessor & µcontroller, Digital processor uses different dedicated hardware architecture; because they have special features real-time operations such as FFT, filtering, convolution & correlations, real time sample based & block based processing.

* The design of general µprocessor & µcontroller is based on Von Neuman architecture; which was developed from a research paper written by Von Neumann & others in 1946.

General µprocessor based on Von Neuman architecture

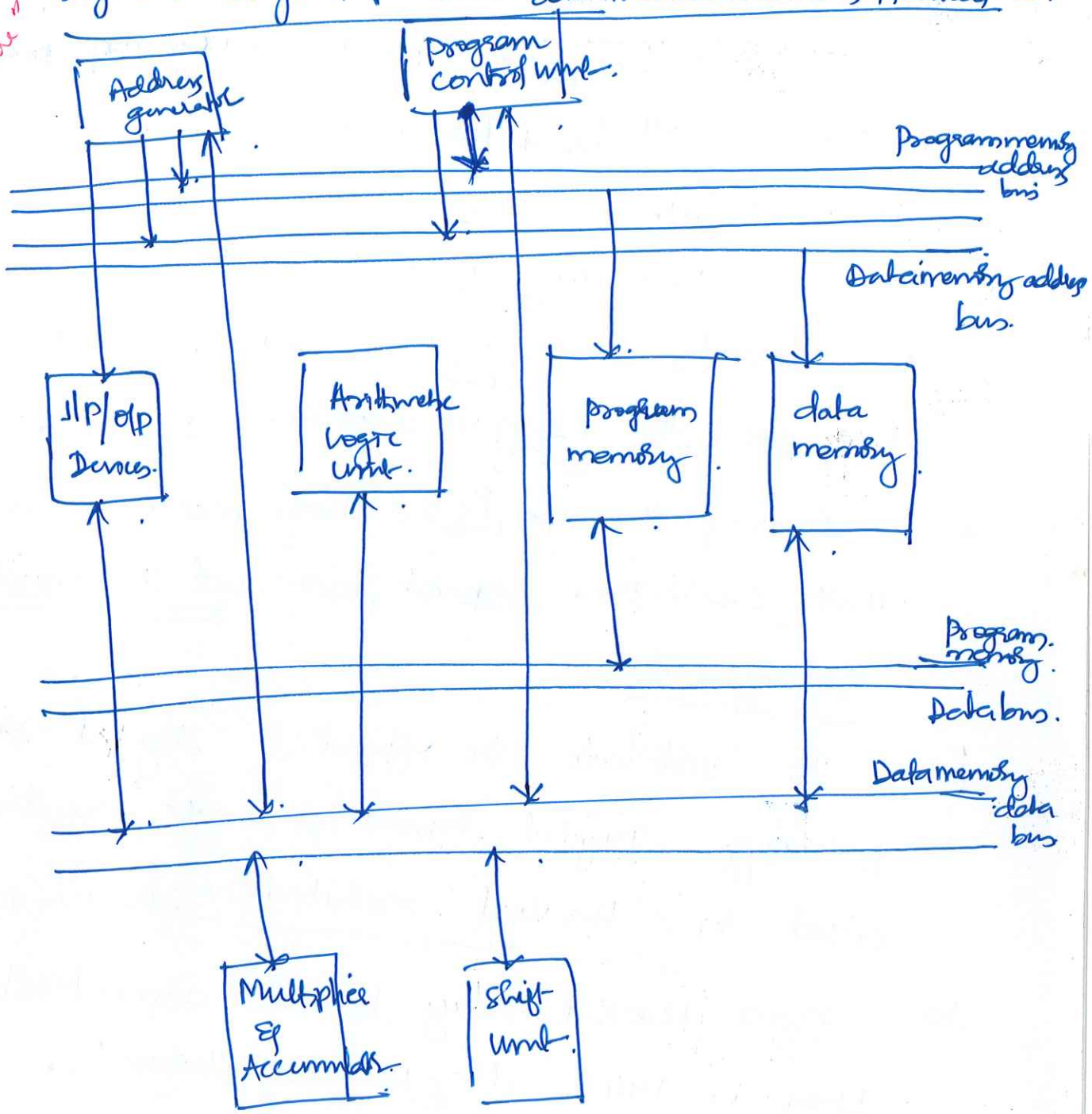


* Von Neuman processor contains a single, shared memory for programs & Data.
* a single bus for a memory access, an arithmetic unit & program control unit.
* the processor proceeds in a serial way in terms of fetching & executing cycles. This means that central processing unit [CPU] fetches an instruction from memory & decodes it into figure out what operations to do, then executes the instructions.
* the instructions has 2 parts, the opcode & the operand.
* the opcode specifies what the operation is. ie tells CPU what to do. the operand informs the CPU what data to operate on. these instructions will modify the memory or I/P & O/P.
* After an instruction is completed, the cycle will resume for the next instruction. one instruction can be retrieved at a time. since the processor proceeds here in a serial fashion, it causes most units to a wait state.
* the Von Neuman architecture operates the cycles of fetching & execution by fetching an instruction from memory, decoding it through program controlling unit & finally executing the instruction.

* When executing requires a data movement, ie data to be read & written to memory, the next instructions will be fetched after the current instruction is completed.
* The Von Neuman based processor has this bottle neck mainly due to use of single, shared memory for both program instructions & data memory.
* Increasing the speed of the bus, memory & computational unit can improve speed but not that much significantly.
* To accelerate the speed of digital signal processing, Digital signal processors are designed based on Harvard architecture: which originated from Mark-I relay based computers built by IBM in 1944 at Harvard University.
* DS. process has 2 seperate memory spaces. one memory is used for program code & the other is used for data.
* Therefore to accomodate 2 memory spaces 2 address buses & 2 data buses are used.
* By this way, the program memory & data memory

Imp
Discuss the Harvard architecture "
(10M)

Digital Signal processor architecture based on Harvard (4)



* have their own connections to the program memory bus & data memory bus respectively.
∴ The Harvard processor can fetch the program instruction & data is parallel at the same time.
* There is an additional unit called Multiplier & accumulator (MAC) which is a dedicated hardware used for ~~digital~~ digital filtering operations.

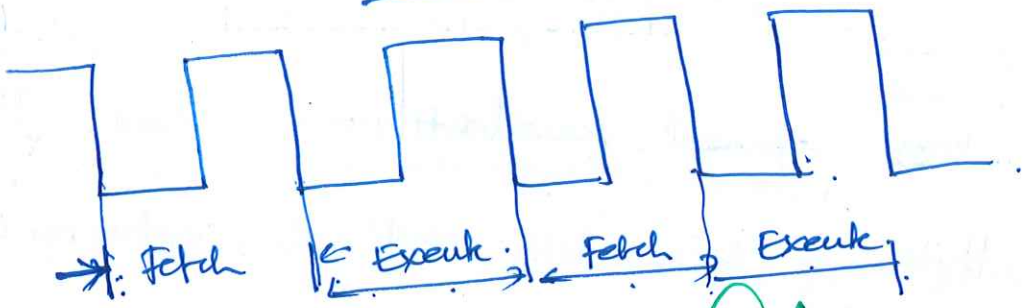
(4)

* the last unfilled shift unit used for the scaling operation for a fixed pt implementation when the processor performs digital filtering..

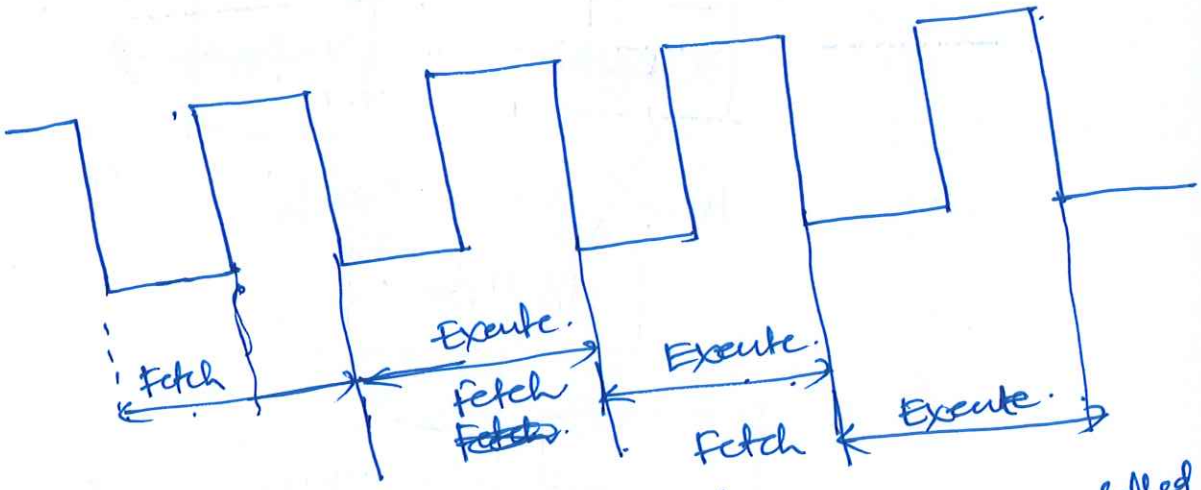
comparisons of executions of 2 architectures.

* . Execution cycle timings of

Harvard Von Neumann.



Harvard



* Execute of fetch cycles are overlapped here → is called Pipelining op"
* Speed of the processor is improved very much here.
* one register holds the filter co-efficients while the other register holds the data to be processed.
*

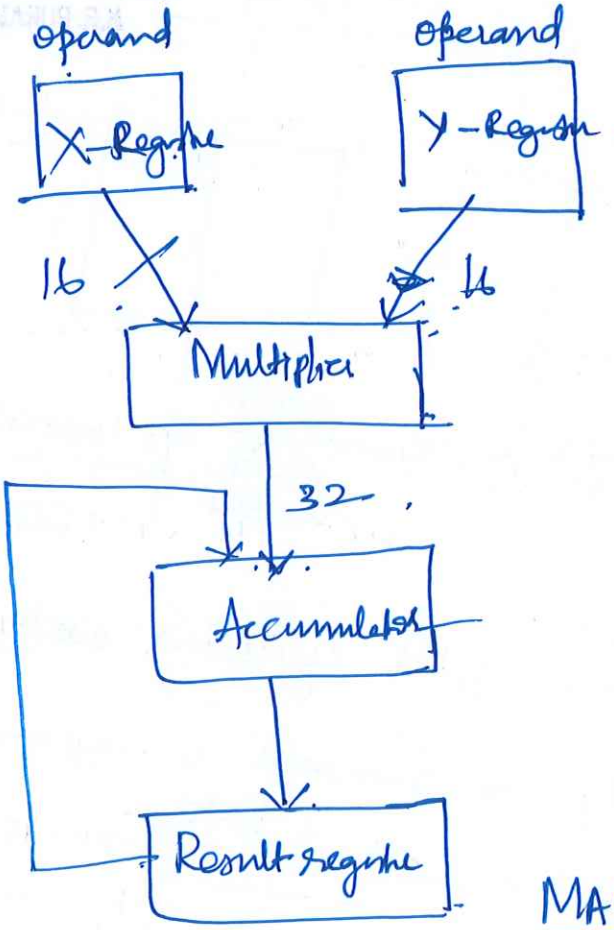
DSP Processor Hardware Units

(10M) Discuss in brief the DSP processor hardware units

* Multiplier Accumulator unit (MAC) unit.
* Shifters
* Address generator

Multiplier & Accumulator unit.

* DSP processor uses special hardware unit called (MAC) Multiplier & Accumulator unit which enhances the speed of digital filtering.



MAC unit.

* Multiplier has a pair of i/p registers, each holding 16 bit i/p to the multiplier,

* The result of the multiplication is accumulated in 32-bit accumulator unit.
* The result register gives the double precision data from the accumulator.

Shifters

* In digital filtering, to prevent overflow a scaling operation is required.
* A simple scaling-down operation shifts data to the right, where as scaling-up operation shifts data to the left.
* Shifting data to the right is same as dividing the data by 2 & truncating the fraction part.
* Shifting data to the left is eq to multiplying data by 2

Ex: Consider 3 bit word, '011' = 3

Shifting data to the right 1 bit (011) = 1

ie $3/2 = 1.5$ truncate 1.5 gives 1.

* Shifting to left 1 bit = $(110)_2 = 6$

ie $3 \times 2 = 6$ ie multiplying data by 2

ie $3 \times 2 = 6$

* The DS processor often shifts data by several bits for each word.

* To speed up such operations, special hardware unit called shifter is designed to do scaling op^n.

Address Generator

[Explain briefly the working of Address generator unit]

** The DS processor generates the addresses for each data in the data buffer to be processed.

** A special hardware unit called Address generator are used for circular buffering.

* In circular buffering, a pointer is used & always points to the newest data sample.

* After the next sample is obtained from Analog to Digital conversion (ADC), the data will be placed at location x(n-7). The oldest sample is pushed out.

* Then the location for x(n-7) becomes the location for the current sample x(n).

* The original location for x(n) becomes a location for the past sample of x(n-1). The process continues like this mechanism.

(8)

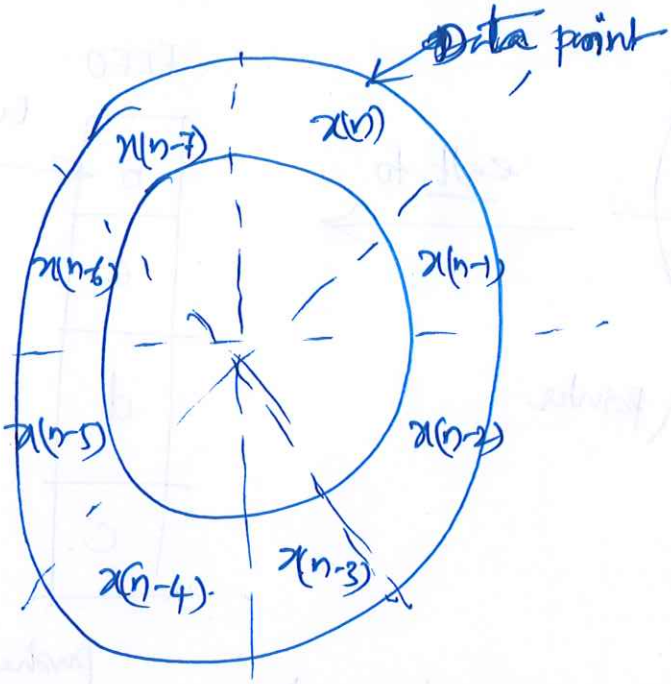
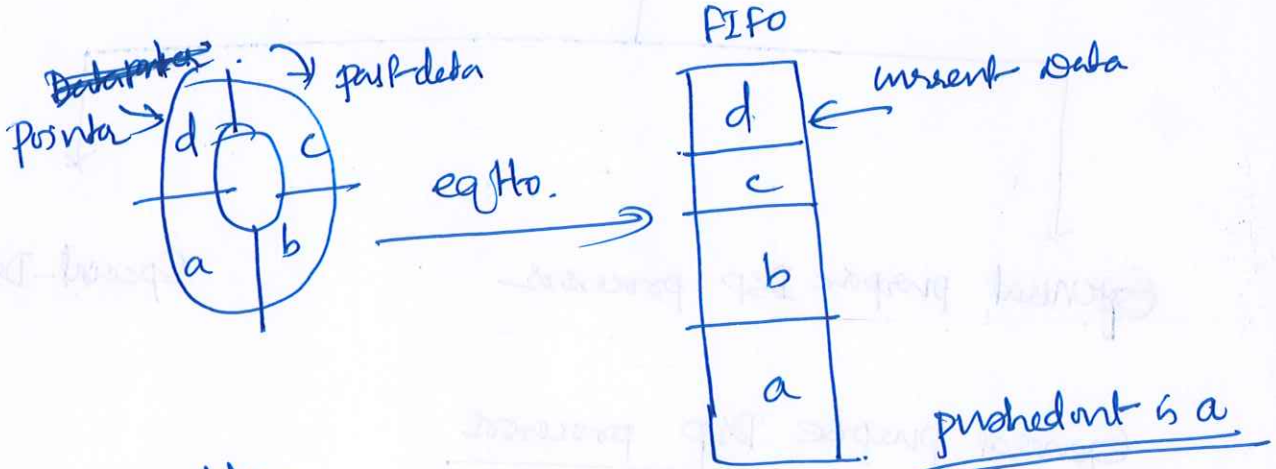
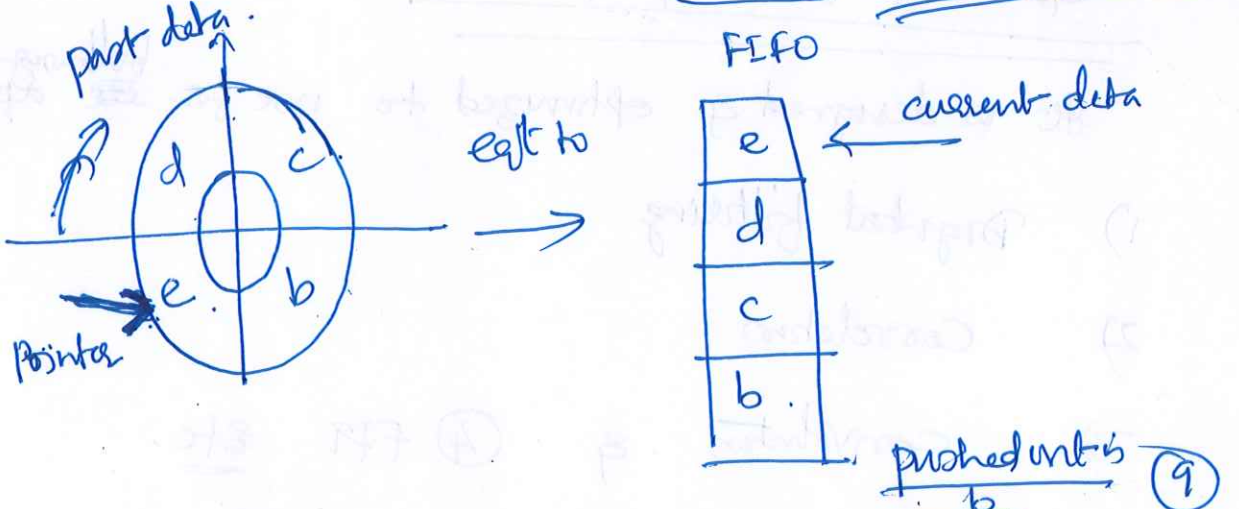


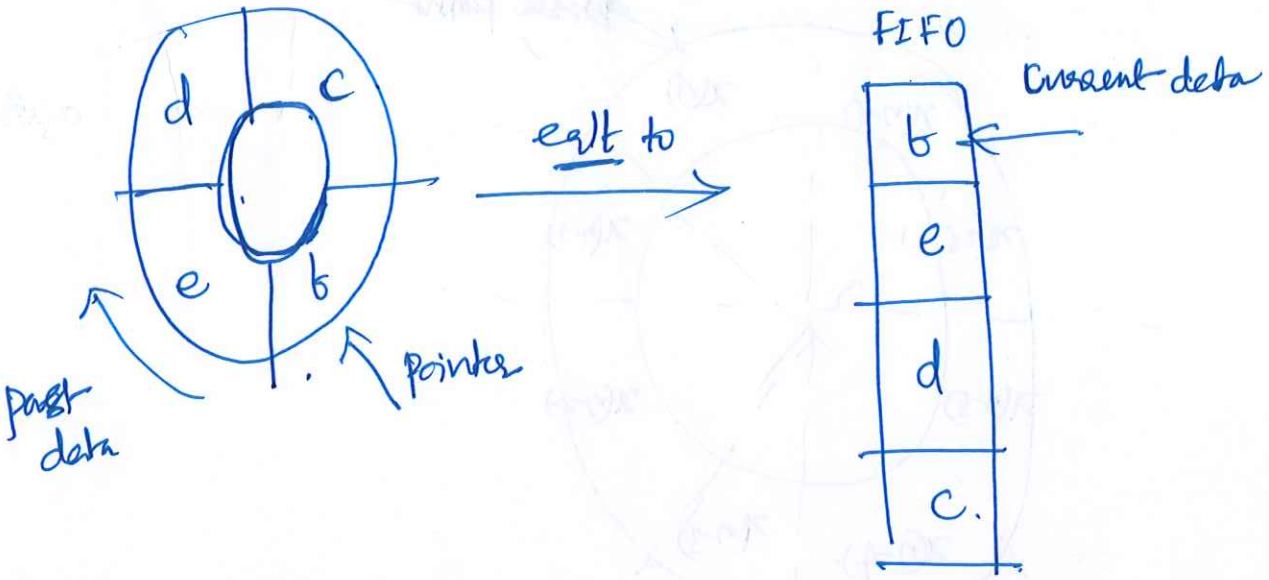
Illustration of circular buffering.

Circular buffer eg eqvt FIFO.

Data flow a, b, c, d, e, f - - - .







Circular buffer & eqt FIFO. diagram

Digital signal processors & Manufacturers

DS processors are classified as

- General purpose DSP processors
- Special-DSP processors.

General purpose DSP processor

It is designed & optimized to use for following applications.

1) Digital filtering
2) Correlation
3) convolution & (4) FFT etc.

Special DSP-processor

It has features that are optimized for unique applications such as

1) Audio processing
2) Compressing.
3) Eco cancellations..
4) Adaptive filtering.

Major manufacturers for DSP are.

1) Texas Instruments (TI)
2) Analog Devices & Motorola - Etc.

Fixed point formats & floating point formats.

* To process real-world data in real time, we need to select correct DS processor & DSP algorithms for particular applications.

* DS processors & uses fixed pt or floating pt techniques depending on how the processor CPU performs arithmetic.

* Differentiate between fixed pt & floating pt processor

* Fixed pt - DS processor	Floating pt = DS processor
* Represents data in 2's complement integer format &	whereas floating point

& manipulates data using integer arithmetic.

processor represents number using a mantissa (fractional part) & an exponent in addition to the integer format.

it operates data using floating point arithmetic

2) since it operates using integer format, it represents only a very narrow dynamic range of integer no.

(2) Represents wider range of data, since it operates using floating-pt formats.

3) coding takes more time because of overflow data problems.

(3) Coding is much easier

4) requires less hardware

4) Requires more hardware

5) less expensive.

5) More expensive

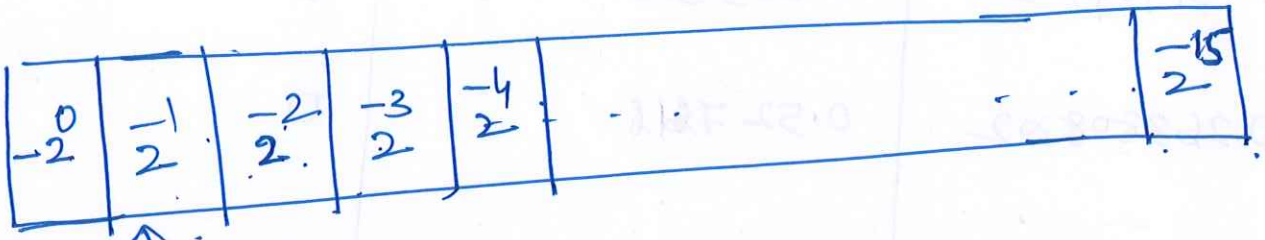
6) it is faster in terms of instruction cycles.

6) it is slower in terms of Instruction cycles.

* Q-format number representation is the most common representation used in fixed-point DSP implementation.

Eg Q-15 (fixed-pt) format.

Q-15



* Q-15 format means the data are in a sign magnitude form in which there are 15 bits for magnitude & 1 bit for sign.

(SM)

Example-1) Find the signed Q-15 representation for decimal no 0.560123.

Converting Decimal no to Q-15 representation

Number	product	carry
0.560123×2	1.120246	1 (MSB)
0.120246×2	0.240492	0
0.240492×2	0.480984	0
0.480984×2	0.961968	0
0.961968×2	1.923936	1
1.923936×2	1.847872	1
0.847872×2	1.695744	1
0.695744×2	1.391488	1

0.391488×2	0.782976	0
0.782976×2	1.565952	1.
0.565952×2	1.131904	1.
0.131904×2	0.263808	0
0.263808×2	0.527616	0
0.527616×2	1.055232	1.
0.055232×2	0.110464	0 (LSB).

* For a positive fractional no, we multiply no by 2. If the product is larger than 1, carry bit '1' is taken as MSB bit.
* If the product is less than 1, carry bit is written as '0'.
* This process is done till all 15 magnitude bits gets over

∴ Q-15 format representation is:

0.1000 1111 0110 010.

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2) Ex-2

Find the signed Q-15 representation for the decimal no.

-0.160123.

Soln

Convert the Q-15 format for corresponding positive no with same magnitude as given by. (15)

Number	Conversion of Q15 format to decimal no. product	carry
0.160123×2	0.320246	0. (MSB)
0.320246×2	0.640492	0.
0.640492×2	1.280984	1.
0.280984×2	0.561968	0
0.561968×2	1.123936	1.
0.123936×2	0.247872	0.
0.247872×2	0.495744	0.
0.495744×2	0.991488	0
0.991488×2	1.982976	1
0.982976×2	1.965952	1
0.965952×2	1.931904	1
0.931904×2	1.863808	1
0.863808×2	1.727616	1
0.727616×2	1.455232	1
0.455232×2	0.910464	0

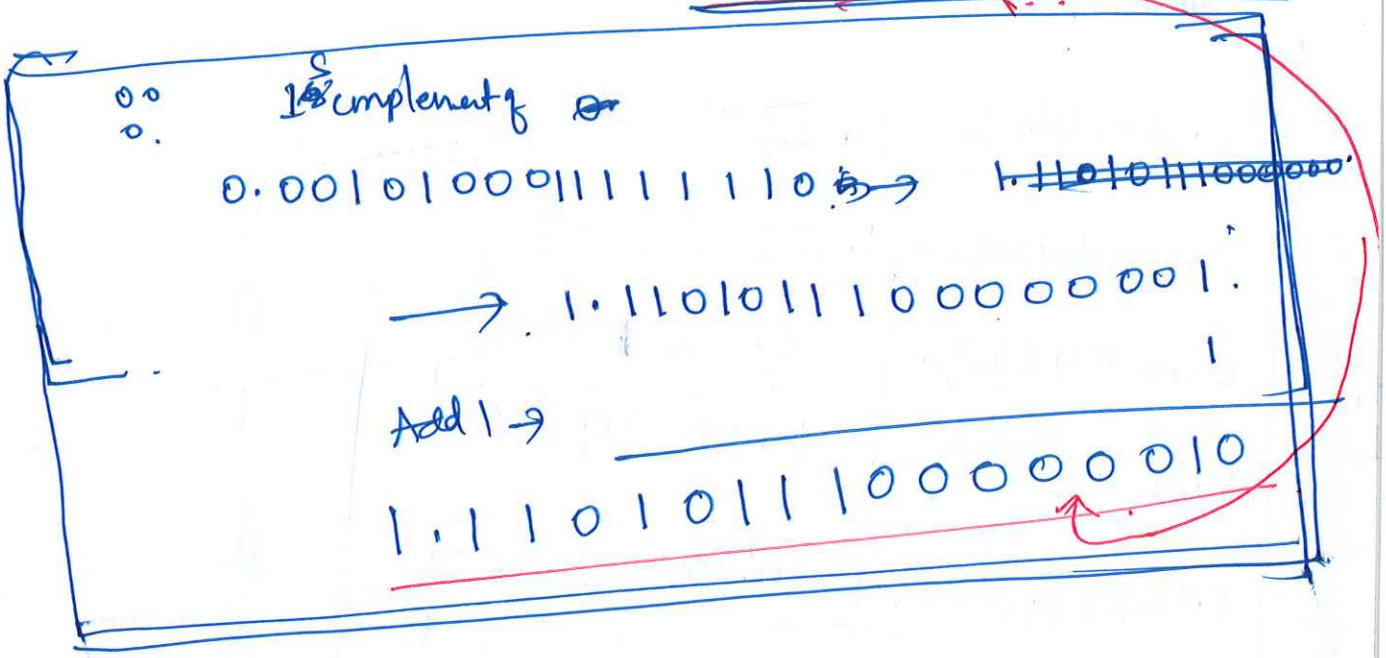
(15)

Q-15 Representation for +ve no is 0.160123 is

$= 0.0010100011111110.$

Q-15 Representation for -ve no after applying 2^s complement is given by

$-0.160123 \longrightarrow 1.1101011100000010.$



(3). Convert Q-15 signed no 1.1101011100000010 to the decimal no.

Soln. Since the nos -ve, Apply 2^s complement weight -

$1.1101011100000010.$

0.0010100011111101 } 2^s complement
$\quad\quad\quad\quad\quad\quad 1$ }.

$\rightarrow$

0.0010100011111110

* The decimal no is

$= (2^{-3} + 2^{-5} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-12} + 2^{-13} + 2^{-14})$ (4)

$= -0.160095$ [Decimal no]

(4) Convert Q-15 Signed no 0.100011110110010 to its Decimal no

Soln Since the given no is +ve no, Directly we can get decimal no.

i.e

$= \left(2^{-1} + 2^{-5} + 2^{-6} + 2^{-7} + 2^{-8} + 2^{-10} + 2^{-11} + 2^{-14}\right)$

$= 0.560120$

(5) Add following 2 Q-15 format & convert it into decimal no.

i.e 0.11010111000000.
0.10001111011010.

Soln Binary addition

```
  1 1 1 1           1
  1.1 1 0 1 0 1 1 1 0 0 0 0 0 0 1 0
  0.1 0 0 0 1 1 1 1 0 1 1 0 0 1 0
 10.0 1 1 0 0 1 1 0 0 1 0 0 1 0 0
```

∴ The result is 0.0110011001001100

∴ Decimal no's

$$= + \left(2^{-2} + 2^{-3} + 2^{-6} + 2^{-7} + 2^{-10} + 2^{-1} + 2^{-13}\right)$$

$$= 0.140024$$

Floating point format

6M

* Write a short note on floating pt format, or.
Discuss floating point format representation.

* Floating point format is used to increase the dynamic range of number representation.

* General format for floating point representation is given by.

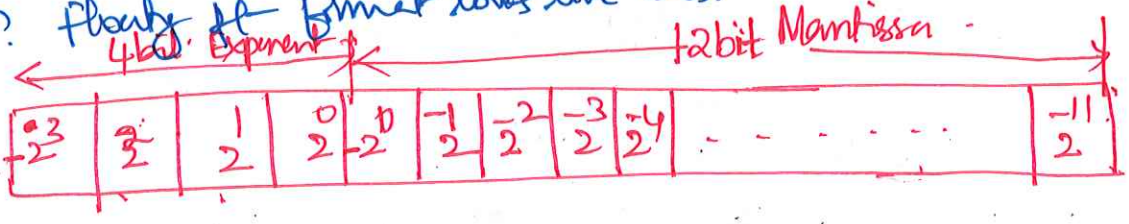
$$x = M \cdot 2^{E} \longrightarrow (1)$$

Where M → is nothing but Mantissa or a fractional part no Q found. &

E → is Exponent.

* the mantissa & exponent are nothing but signed numbers.

* we assign 12 bits to mantissa & 4 bits to exponent then floating pt format looks like this.



* Since 12 bit Mantissa is limited between -1 & +1.

the no of bits assigned to the exponents controls the dynamic range.

* bigger the no of bits designated to the exponent the larger the dynamic range.

* the no of bits for the mantissa defines the interval in the normalized range.

* the interval size shown above is 2^{-11} comes in the normalized range, which is smaller than Q-15 format.

* most -ve & most +ve nos are defined as.

most -ve no. = $(1.000000000000)_2 * 2^{0111_2}$ (4 bit.)
(12 bits.)

$= (-1) \times 2^7$

$= -128.0$

most +ve no = $(0.000000000000)_2 * 2^{0111_2}$

$= (1 - 2^{-11}) \times 2^7 = 127.9375$

IEEE Floating-pt formats

(**6M)

* Discuss- IEEE floating pt format (single precision format or Double precision format.

* IEEE floating pt format are commonly used in

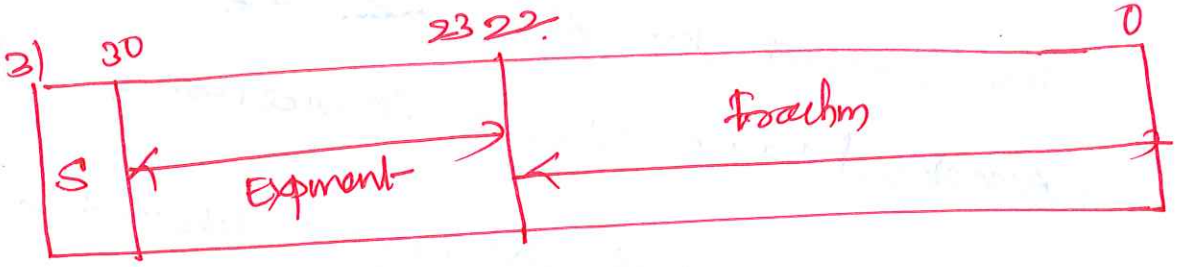
modern DS processor

* They are of 2 types of format.

1) Single precision IEEE floating pt format
2) Double precision IEEE floating pt format.

Single precision IEEE floating pt format.

* The format of single precision is given by.



* The formula used to convert IEEE single precision format to decimal is given by

$$x = (-1)^{S} (1 \times F) \times 2^{E-127}$$

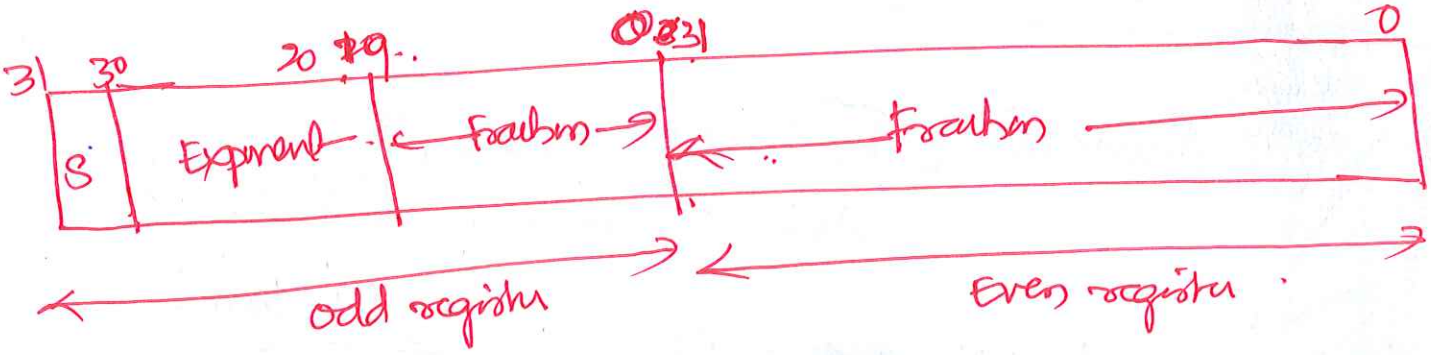
* the format requires 23 bits as fractional bits indicated by F.
* 8 bits as exponential bits.
* 1 bit as sign bits.. with a total of 32 bits for each word.
* F is the mantissa in 2's complement positive

binary fractions represented from bit 0 to bit 22.

* the mantissa is within the normalized range between +1 & +2.
* Sign bit S indicates the sign of a no.
* if S=1 the no is -ve
  S=0 the no is +ve.
* the Exponent 'E' is in Excess 127 form.
* the value of 127 is the offset from the 8 bit Exponent range from 0 to 255. So val. E-127 will have range from -127 to 128.

Double-precision format

* the format is shown below.



* the formula used to convert Double precision format to decimal no is

$$x = (-1)^S * (1 * F) \times 2^{E-1023}$$

* Double precision format requires 64 bit word for representation.
* It vary from 0 to 63. Right to left.
* The first bit is called Sign bit indicated by 'S'
* next 11 bits are called Exponential bit indicated by 'E'
* Final 52 bits are called fractional bits indicated by 'F'.
* The IEEE format in double precision significantly increases the dynamic range of number representation. Since there are 11 Exponential bits.
* It reduces the interval size in the mantissa normalized range of +1 to +2, since there are 52 mantissa bits compare to 23 bits in case of Sigle precision format.

Architecture of Dsp fixed pt processor, Floating pt processor } study from "Li Tan".

Available in library.

All the best students.